2019

Basic Electronics

1. **Answer any seven of the following questions:**

(a) Clipper and clamper are the applications of ....

Ans. Diodes

(b) Give one application of zener diode.

Ans. Zener diodes are used for voltage regulation, as reference elements, surge suppressors, and in switching applications and clipper circuits.

(c) SCR is bistable device.

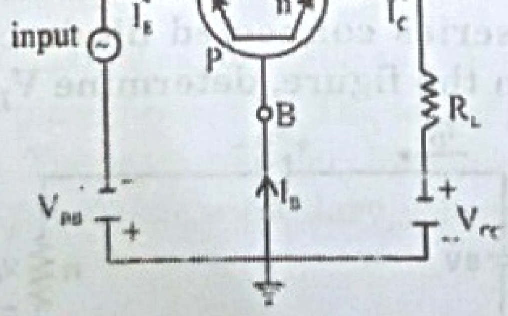
Ans. A thyristor functions as a bistable switch, which means that it starts con- ducting when its gate receives a pulse of current. It conducts until the voltage in the device reverses, i.e., until it is in the forward biased state. Thyristors only turn off when the forwar current drops to zero.

(d) Which of the transistor currents is always the largest ?

Ans. The emitter current IE is always the largest one. The base current IB is always the smallest. The collector current IC and emitter current IE are relatively close in magnitude.

(e) Sketch the common-base BJT transistor configuration (for n-p-n and p-n-p).

Ans. In this, the input signal is given to base & emitter and output is taken across collector and base. Thus it becomes common base as shown.



Here $\quad I_C = \propto I_E + I_{CBO}$

Where, $\propto$ = current amplification factor

I_E = emitter current

I_{CBO} = Leakage current in output circuit.

(f) Why is coupling capacitor used in common-emitter amplifier ?

Ans. In Common Emitter Amplifier circuits, capacitors C1 and C2 are used as Coupling Capacitors to separate the AC signals from the DC biasing voltage.

(g) Which BJT amplifier configuration has unit voltage gain?

Ans. As the voltage gain of the common base amplifier is dependant on the ratio of these two resistive values, it therefore follows that there is no phase inversion.

(h) Which BJT amplifier ?

Ans. There are three basic BJT amplifier configurations that are generally identified as: common- emitter, common-base, and common-collector (sometimes called the emitter-follower). Each of these configurations exhibit certain characteristics that make them more desirable in certain circuit applications than the others.

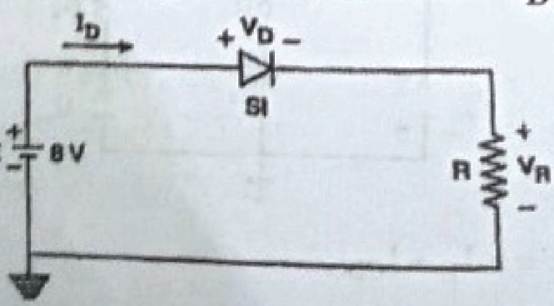
(i) Define convesion efficiency.

Ans. Energy conversion efficiency (n) is the ratio between the useful output of an energy conversion machine and the input, in energy terms.

(j) What is the highest efficiency of class A direct coupled amplifier ?

Ans. The theoretical maximum efficiency of a Class A power amplifier is 50%. In practice, with the capacitive coupling and inductive loads (loudspeak- ers), the efficiency can decrease as low as 25%. This means 75% of power drawn by the amplifier from the supply line is wasted.

Q.2. (a) For the series connected diode configuration as given below in the figure, determine V_D, V_R and I_D:



Ans. $V_D = 0.7$ volts

$E = 0.7 + I_D R$

$$I_D = \frac{8-0.7}{R} = \frac{8.3}{R} A$$

$V_R = 8 - 0.7 = 7.3$

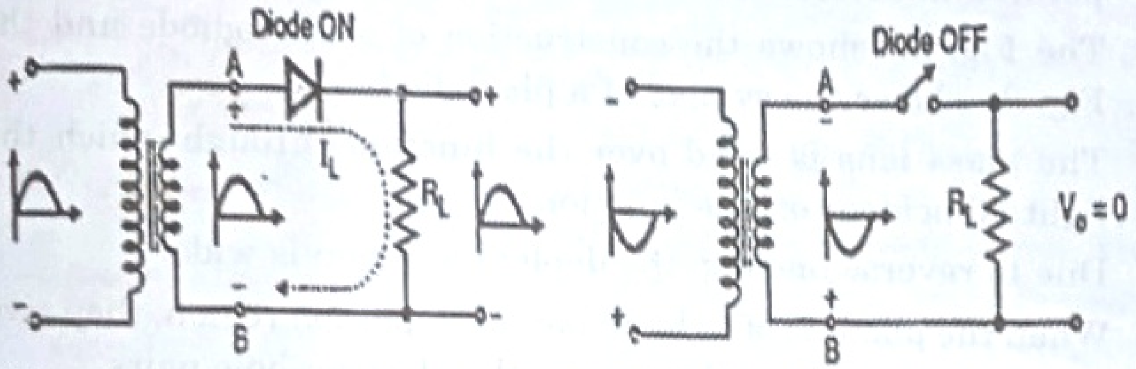
(b) Draw the diagram and explain the working of a full-wave rectifier with filter.

Ans. Operation(working) of the HWR.

The operation of HWR circuit is as follows:

Operation in the positive half cycle of ac supply (0-π):

- In the positive half cycle (0-π) of the ac supply, the secondary voltage V_{AB} is positive. i.e. A is positive with respect to B. Hence the diode is forward biased and starts conducting.



(a) Equivalent circuit for half cycle (b) Equivalent circuit for negative half cycle

- The equivalent circuit of HWR for the positive half cycle is shown in Fig. (a). As the diode starts conducting, the secondary voltage V_{AB} appears almost as it is across the load resistance (as the voltage drop across a conducting diode is very small).
- The load voltage is thus positive and almost equal to the instantaneous secondary voltage V_{AB}.
- The load current has the same shape as that of the load voltage since the load is purely resistive. The waveforms for HWR are shown in Fig.(a). The instantaneous load current i_L is equal to the ratio of instantaneous secondary voltage (V_{AB}) and total resistance ($R_S + R_F + R_1$).

$$I_L = \frac{V_{AB}}{(R_S + R_F + R_L)} \quad \text{.................... (1)}$$

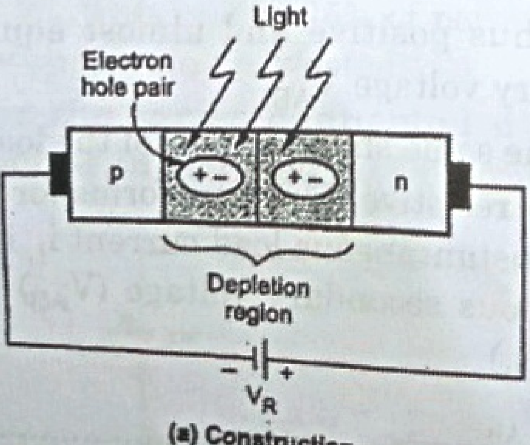
Operation in the negative half cycle of ac supply (π to 2π)

- Refer to the equivalent circuit shown in Fig.(b). In the negative half cycle of the ac supply $(\pi \text{ to } 2\pi)$, secondary voltage V_{AB} is negative i.e. A is negative with respect to B.
- Hence the diode is reverse biased and offers a very high resistance.
- Hence we can replace it by an open circuited switch.
- The load is disconnected from the secondary. Hence the load voltage and load current both are zero and the voltage across the diode is equal to the instantaneous secondary voltage V_{AB} The waveforms are shown in Fig. (a).

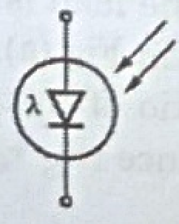
Q.3. (a) Explain the working and applications of photodiode.

Ans. The photodiode is a semiconductor p-n junction which is always perated in reverse biased condition.

- The Fig. (a) shows the construction of a photodiode and the Fig. (b) shows the symbol of a photodiode.
- The glass lens is fixed over the junction through which the light is incident on the junction.
- Due to reverse biasing, the depletion region is wide.
- When the photons of light strike the depletion region, they give energy to the ions and generate the electron-hole pairs.
- The number of electron-hole pairs depend on the intensity of the light. Due to increased minority carriers, the reverse current increases, which is nothing but a photocurrent.
- More the light intensity, more is the number of electron-hole pairs and more is the photocurrent.



(a) Construction



(b) Symbol

Fig. Photodiode

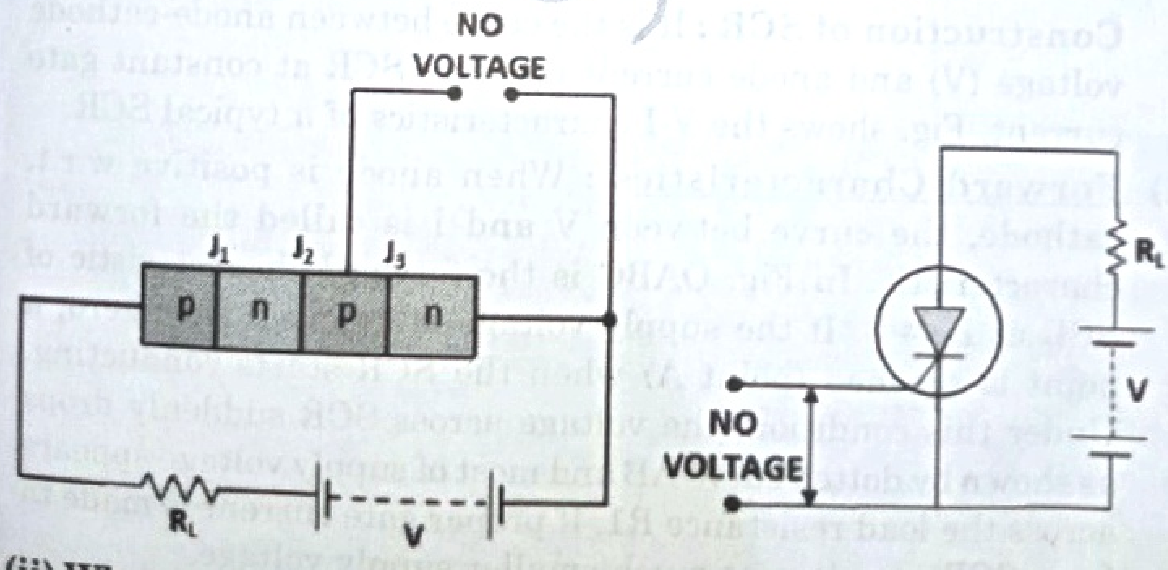
Application of photo diode :

Photodiodes are used in safety electronics such as fire and smoke detectors. Photodiodes are used in numerous medical applications. They are used in instruments that analyze samples, detectors for computed tomography and also used in blood gas monitors. Photodiodes are used in solar cell panels.

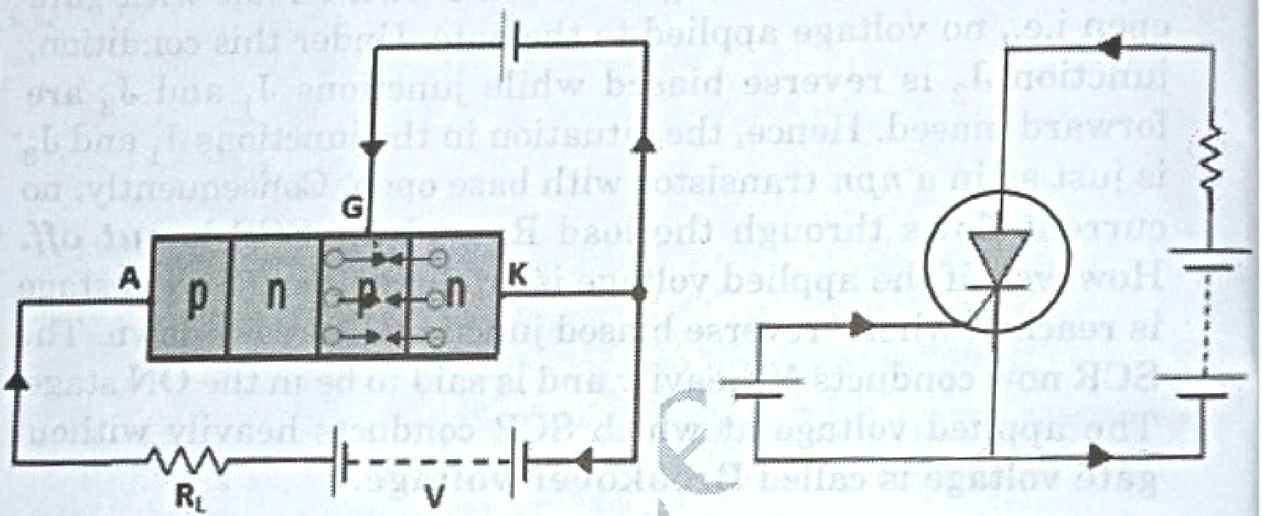
Q.3. (b) Explain the construction, operation and characteristics of SCR.

Ans. In a silicon controlled rectifier, load is connected in series with anode. The anode is always kept at positive potential w.r.t cathode. The Operational (working) of SCR can be studied under the following two heads :

(i) When gate is open : Fig. shows the SCR circuit with gate open i.e., no voltage applied to the gate. Under this condition, junction J_2 is reverse biased while junctions J_1 and J_3 are forward biased. Hence, the situation in the junctions J_1 and J_3 is just as in a *npn* transistor with base open. Consequently, no current flows through the load R_L and the SCR is ***cut off.*** However, if the applied voltage is gradually increased, a stage is reached when *reverse biased junction J_2 breaks down. The SCR now conducts ** heavily and is said to be in the ON stage. The applied voltage at which SCR conducts heavily without gate voltage is called **Breakover voltage.**



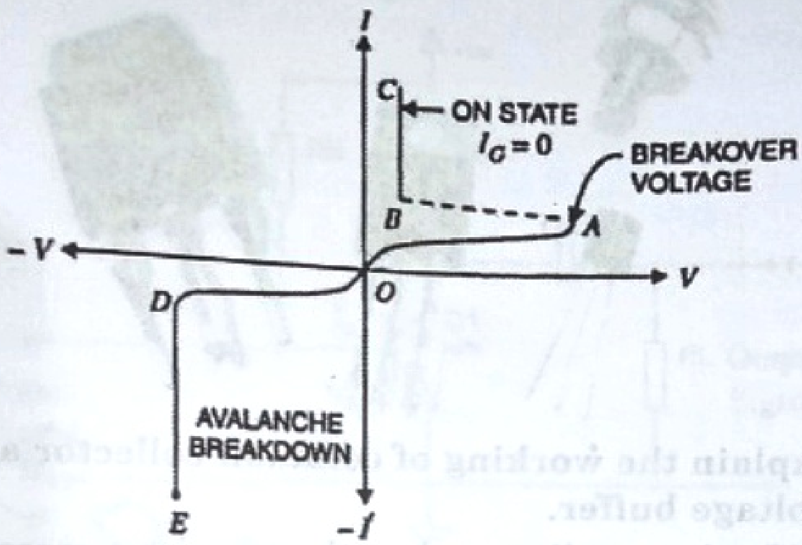
(ii) When gate of positive w.r.t cathode: The SCR can be made to conduct heavily at smaller applied voltage by applying a small positive potential to the gate as shown in Fig. Now junction J_3 is forward biased and junction J_2 is reverse biased. The electrons from *n*-type material start moving across junction J_3 towards left whereas holes from *p*-type towards the right. Consequently, the electrons from junction J_3 are attracted across junction J_2 and gate current starts flowing. As soon as the gate current flows, anode current increases. The increased anode current in turn makes more electrons available at junction J_2. This process continues and in an extremely small time, junction J_2 breaks down and the SCR starts conducting heavily. **Once SCR starts conducting, the gate** (the reason for this name is obvious) loses all control. Even if gate voltage is removed, the anode current does not decrease at all. The only way to stop conduction (i.e., bring SCR in off condition) is to reduce the applied voltage to zero.



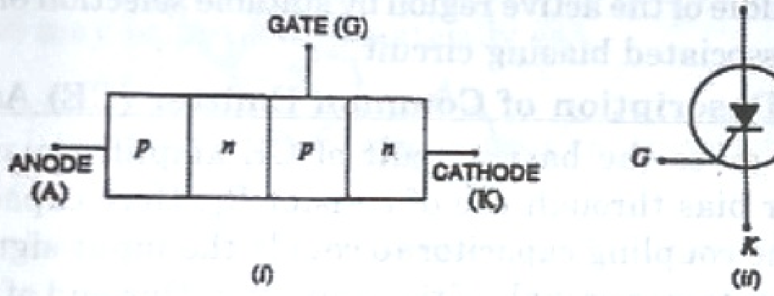
Construction of SCR : It is the curve between anode-cathode voltage (V) and anode current (I) of an SCR at constant gate current. Fig. shows the V-I characteristics of a typical SCR.

(i) **<u>Forward Characteristics</u>** : When anode is positive w.r.t. cathode, the curve between V and I is called the forward characteristic. In Fig. OABC is the forward characteristic of SCR at $I_G = 0$. If the supply voltage is incrased from zero, a point is reached (point A) when the SCR starts conducting. Under this condition, the voltage across SCR suddenly drops as shown by dotted curve AB and most of supply voltage appears across the load resistance R1. If proper gate current is made to flow, SCR can close at much smaller supply voltage.

(ii) **<u>Reverse Characteristics</u>** : When anode is negative w.r.t. cathode, the curve between V and I is known as reverse characteristic. The reverse voltage does come across SCR when it is operated with a.c. supply. If the reverse voltage is gradually increased, at first the anode current remains small (i.c., leakage current) and at some reverse voltage, avalance breakdown occurs and the SCR starts conducting heavily in the reverse direction as shown by the curve DE. This maximum reverse voltage at which SCR starts conducting heavily is known as ***reverse breakdown voltage.***

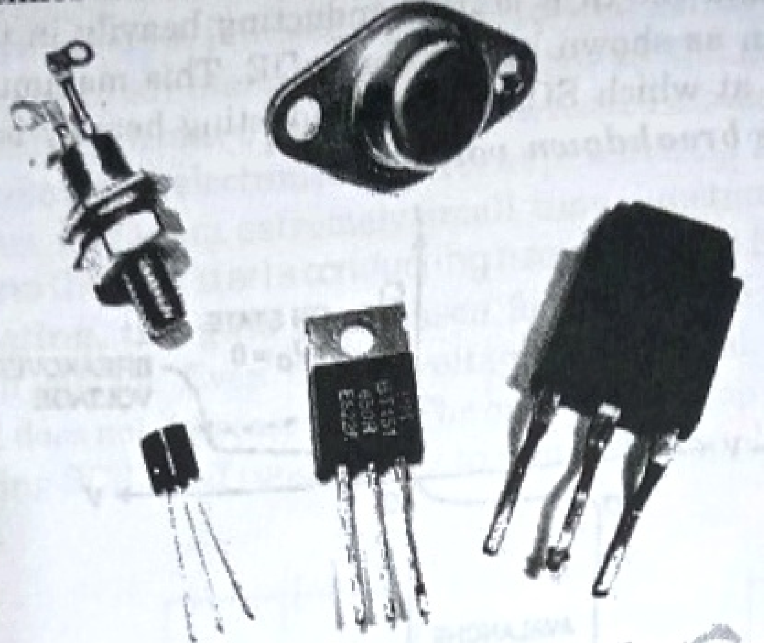


V-I characteristics of SCR :



<u>Constructional Details</u> : When a pn junction is added to a junction transistor, the resulting three pn junction device is called a silicon controlled rectifier. Fig. 1 (i) shows its construction. It is clear that it is essentially an ordinary rectifier (*pn*) and a junction transistor (*npn*) combined in one unit to form ***pnpn device***. Three terminals are taken; one from the outer *p-type* material called anode A, second from the outer *n-type* material called ***cathode*** K Scann and the third from the base of transistor section and is called gate G. In the normal operating conditions of SCR, ande is held at high positive potential w.r.t. cathode and gate at small positive potential w.r.t. cathode. Fig. (ii) shows the symbol of SCR.

The silicon controlled rectifier is a solid state equivalent of thyratron. The gate, anode and cathode of SCR correspond to the grid, plate and cathode of thyratron. For this reason, SCR is sometimes called thyristor.



Q.4. (a) Explain the working of common-collector amplifier as a voltage buffer.

Ans. Amplifier is most linear when the transistor operates in its active region. Hence the operating point must be suitably placed in the middle of the active region by suitable selection of external energy associated biasing circuit.

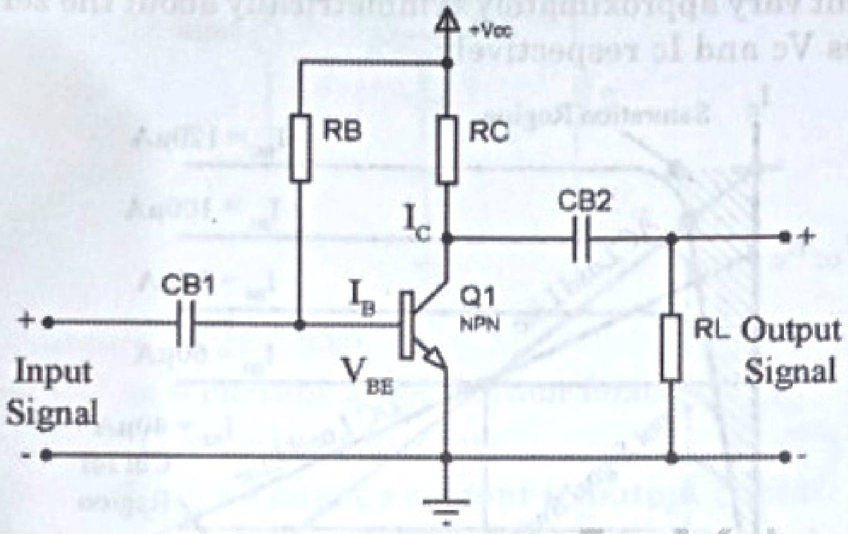
Circuit Description of Common Emitter (CE) Amplifier

Figure 1 gives the basic circuit of CE amplifier using NPN transistor bias through use of resistor R_b. Here capacitor C_{b1}, acts as the coupling capacitor to couple the input signal to the base-to-emitter terminals of the transistor. One end of the input voltage Vi is at the ground potential. Vcc is the collector supply voltage which serves the additional function of providing the bias current I_B. Under zero signal condition, C_{b1} acts as an open circuit since the reactance of a capacitor is infinity at zero frequency (dc).

Thus, the capacitor C_{b1} acts as blocking capacitor. Normally C_{b1}, is chosen so large that at the lowest signal frequency, its reactance is small enough to be considered as a short circuit. Thus, capacitor C_{b1} blocks dc voltage but passes a.c. signal voltage. Similarly, capacitor C_{b2} serves the same two functions. Thus, C_{b2} works as coupling capacitor and feeds the amplified a.c. signal to constitute the output voltage V_0 across R_L. Simultaneously C_{b2} blocks the d.c. voltage. Thus, the amplified output a.c. voltage may be applied to the input of the next amplifier stage without affecting the bias of the next stage.

DC and AC Load Lines | Common Emitter (CE) Amplifier

For given collector characteristics and transistor biasing, selection of proper operating point involves selection of suitable values of Rc and V_{cc}.



CE Amplifier with Fixed Bias

Collector current Ic is a function of VCE and base bias current IB and may be put mathematically as,

$$I_C = f(V_{CE}, I_B) \quad \text{.........(1)}$$

Equa. 1 represents the static output characteristic of the CE transistor for base current I_B.

On applying Kirchhoff's voltage law (KVL) to the collector circuit including only R_C. (excluding C_{b2} and R_L) We get,

$$V_{CC} = I_C R_C + V_{CE} \quad \text{.........(2)}$$

Equation 2 represents a straight line having intercept Vcc on the voltage axis and intercept $\frac{V_{CC}}{R_C}$ on the current axis. The slope of this line equals $\frac{-1}{R_C}$.

This line is referred to as the load line and represents the dynamic characteristic of the device. The zero-signal operating point must be suitably located on this load line. This, in turn, depends on the value If R_L. If $RL = \infty, R_L$ can be neglected and then for large symmetrical input signal (base current in this case), the operating point P_1 should be located in the centre of the dc load line. V_c and I_c are the zero-signal collector voltage and collector current respectively at the operating point. Next on application of a time varying signal, base current varies symmetrically on either side of I_{B1} the point of operating moves along dc load line symmetrically about the zero-signal operating point P_1 and the instantaneous collector voltage and collector current vary approximately symmetrically about the zero-signal values Vc and Ic respectively.

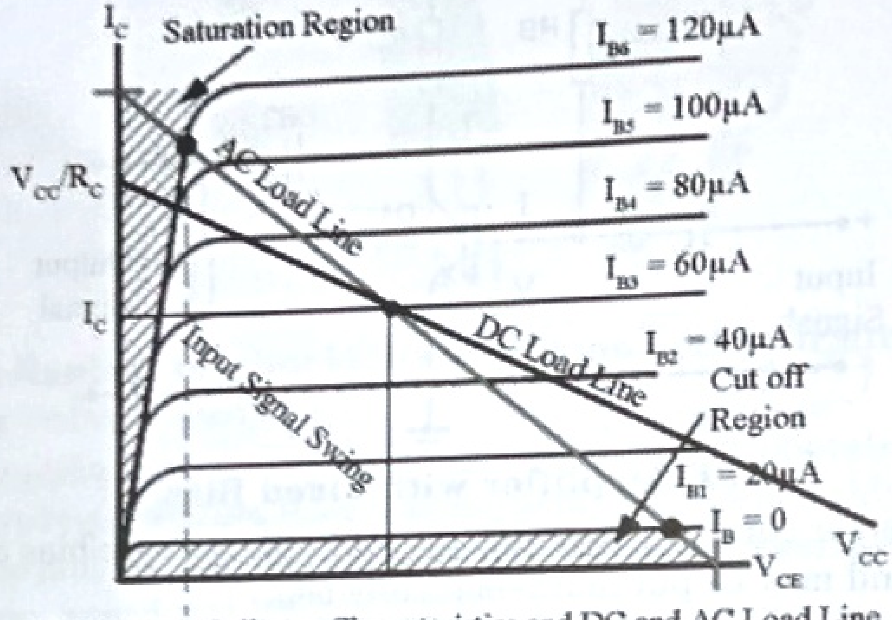


Figure 2: CE Collector Characteristics and DC and AC Load Line

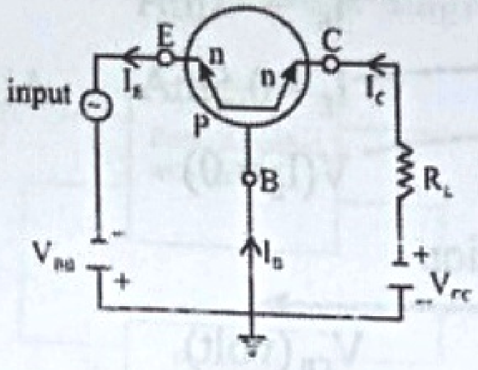
Q.5. (a) Compare between depletion type MOSFET and enhancement type MOSFET.

Ans.

Enhancement MOSFET	Depletion MOSFET
1. It is Normally OFF device at zero Gate to Source voltage.	1. It is Normally ON device at zero Gate to Source voltage
2. At OFF condition it cannot conduct electrical current.	2. At OFF condition it can conduct electrical current.
3. Positive gate voltage (more than source volt- age) is required to turn on this type of MOSFET	3. Negative gate voltage(less than threshold voltage) is required to turn off this type of MOSFET
4. In this type of MOSFET, the gate voltage directly proportional to the Drain Current.	4. In this type of MOSFET, the gate voltage Inversely proportional to the Drain Current.
5. There is no permanent channel; a temporary channel is produced when	5. There is a permanent fabricated channel available. Generally, the N-Type channel

Q.5. (b) Explain the working of common-base amplifier as a current buffer.

Ans. Common Base Configuration :- In this, the input signal is given to base & emitter and output is taken across collector and base. Thus it becomes common base as shown.



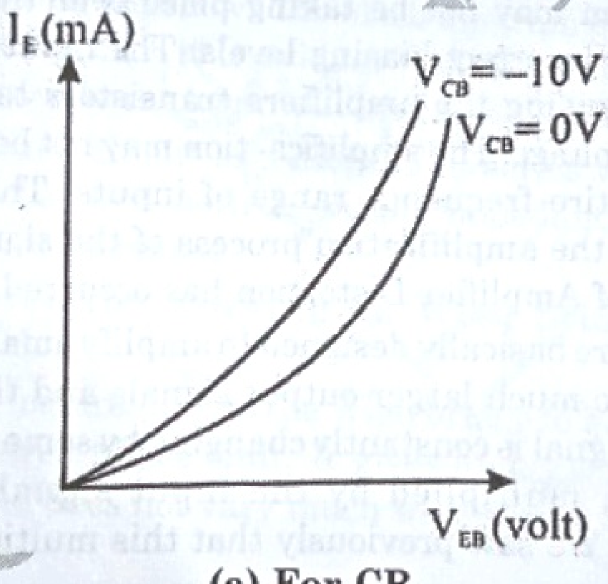
Here $I_C = \propto I_E + I_{CBO}$

Where, $\propto$ = current amplification factor

I_E = emitter current

I_{CBO} = Leakage current in output circuit.

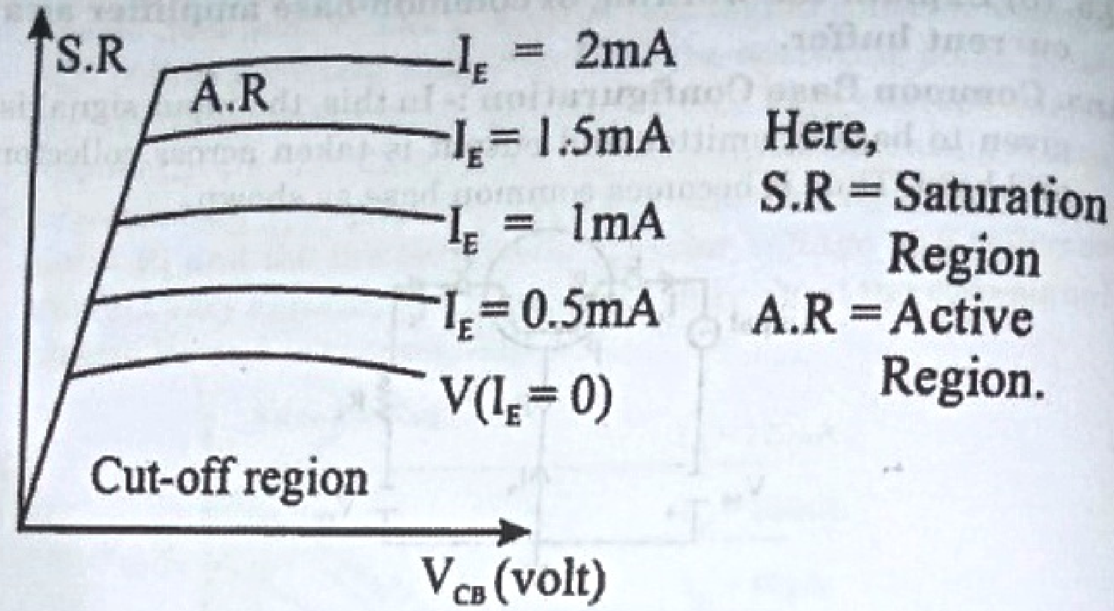
Input characteristics of CB :- It is plotted graph between I, & VEB. Its input characteristics is as shown,



(a) For CB

This is similar to the graph of v-i of forward diode. Here we see that when V_{EB} is increased then I_E is also increased rapidly.

Output characteristics of CB :- It is plotted graph between I_C (output current) and V_{CB} (output voltage).



From output characteristics graph, it is clear that for law value of V_{CB}, I_C changes rapidly when V_{CB} or I_E is increased. In AR, I_C is almost constant.

Q.6. (a) Explain about the distortions present in amplifier. List the advantages of negative feedback.

Ans. Distortion of the output signal waveform may occur because: Amplification may not be taking place over the whole signal cycle due to incorrect biasing levels. The input signal may be too large, causing the amplifiers transistors to be limited by the supply voltage. The amplifica- tion may not be a linear signal over the entire frequency range of inputs. This means then that during the amplification process of the signal wave form, some form of Amplifier Distortion has occurred.

Amplifiers are basically designed to amplify small voltage input sig- nals into much larger output signals and this means that the output signal is constantly changing by some factor or value, called gain, multiplied by the input signal for all input frequencies. We saw previously that this multiplication factor is called the Beta, β value of the transistor. **Advantages of a negative feedback amplifier:**

(1) The negative feedback reduces the size.
(2) It has highly stabilized gain.
(3) It has fewer harmonics distortion.
(4) It has less phase distortion.
(5) It has higher fidelity.

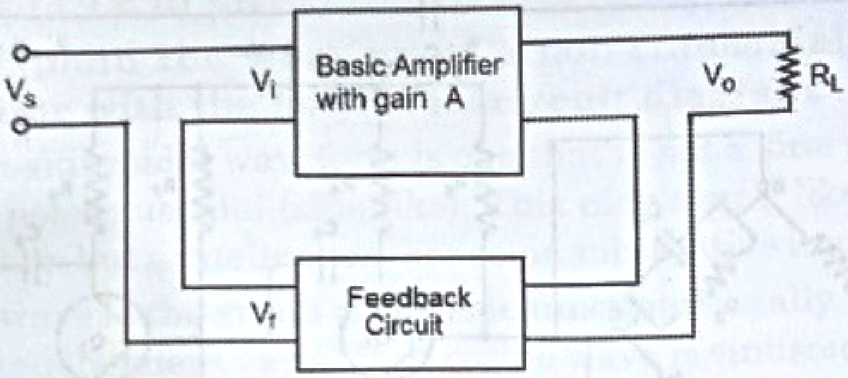
(6) More linear operation.

(7) It has less frequency distortion.

(8) Input-output impedances can be modified as desired.

Q.6. (b) Explain the working of current series feedback amplifier with the help of block diagram.

Ans.



Current-Series Feedback: In the current series feedback circuit, a fraction of the output voltage is applied in series with the input voltage through the feedback circuit. This is also known as series-driven series-fed feedback i.e., a series-series circuit.

The following figure shows the block diagram of current series feed- back, by which it is evident that the feedback circuit is placed in series with the output and also with the input.

As the feedback circuit is connected in series with the output and the input as well, both the output impedance and the input impedance are increased.

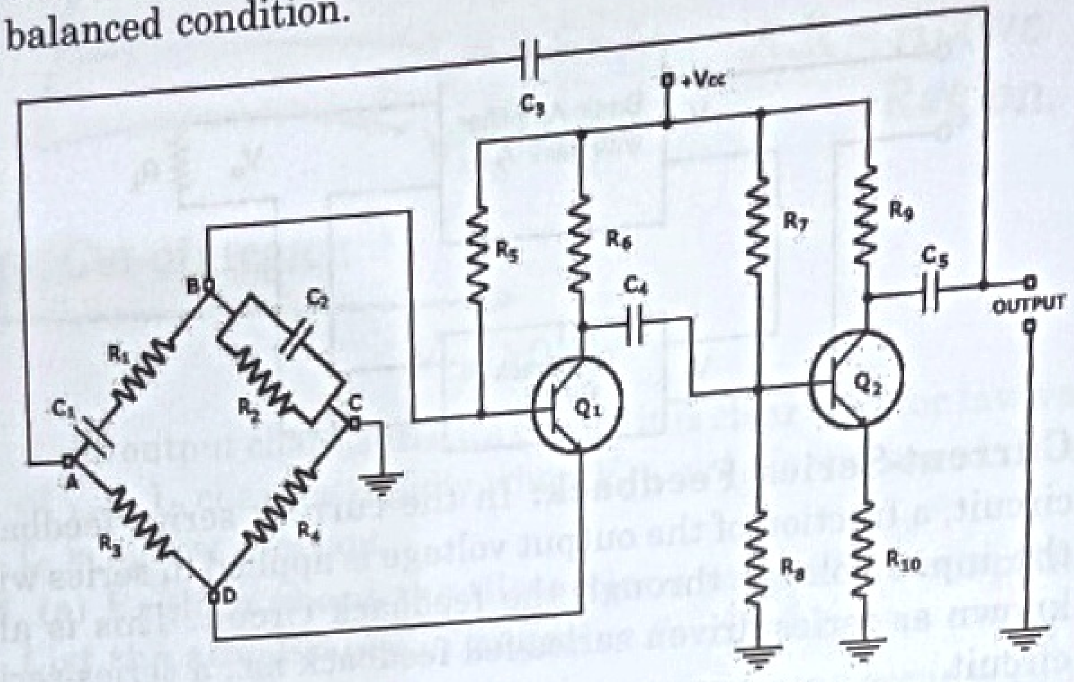
Q.7. (a) Describe the working of Wien bridge oscillator circuit.

Ans. This oscillator circuit uses the Wien bridge to provide feedback with the desired phase shift. It gives highly stable oscillation frequency and does not vary much with supply or temperature variation.

It is basically a two-stage amplifier that consists of an RC bridge circuit or we can say Wien bridge circuit. The Wien bridge feedback net- work is used so as to make the oscillator sensitive to signal of only a particular frequency.

At this particular frequency, the Wien bridge gets balanced and pro-vide's a phase shift of 0°. If Wien bridge feedback is not employed, then it will lead to poor frequency stability due to direct coupling. The Wien bridge circuit that we use is a lead-lag network as with the rise in fre- quency phase shift lags and with the reduction in frequency, it leads.

1 MHz is the maximum output frequency that is provided by this oscillator circuit. In a bridge circuit, the output produced will be in phase with the input only when the bridge is in the balanced condition.



Wien Bridge Oscillator Circuit Diagram

Construction of Wien Bridge Oscillator : Now, let's have a look at the circuit diagram of Wien bridge oscillator. The circuit mainly comprised of two transistors Q_1 and Q_2 and Wien bridge circuit in which a series RC circuit comprising of R_1C_1 is connected with a parallel RC circuit consist- ing of R_2C_2.

At low-frequency range, the reactance of serially connected capacitor C_1 is very high due to which it acts as an open circuit that results in blocking of an input signal which resultantly gives no signal at the output.

Similarly, at a higher frequency, the reactance of parallel capacitor C_2 becomes very low thus behaving like a short circuit across the output, which again results in no signal at the output. So, there is a need to choose a frequency point in between the above two conditions that we have discussed right now so that we can achieve the maximum value at the output.

Q.7. (b) Design the R-C elements of a Wien bridge oscillator, when it operates at f_0 = 10 kHz.

Ans. In oscillation case $R_1 = R_2$, $C_1 = C_2$

Resonant frequency $f_0 = \frac{1}{2\pi R_C}$

$$RC = \frac{1}{2\pi(10\times10^3)} = \frac{7}{440}\times10^{-3} = 15.9\times10^{-6}$$

$R = 1.59 \times 10^{-6}/C$ and

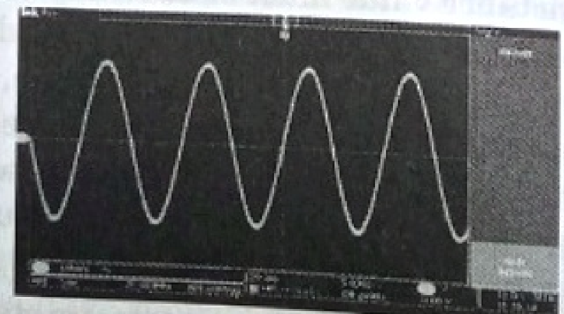
$C = 15.9 \times 10^{-6}/R$

Q.8. (a) Explain the working of a non-sinusoidal type of oscillator with the help of its circuit diagram.

Ans. A non-sinusoidal waveform is one that is not a sine wave and is also not sinusoidal (sine-like). This may sound like a minor distinction but actually there are some substantive implications. A sine wave is the graph of the sine function, usually with time as the independent variable. A cosine wave is sinusoidal. It has the same form but it has been phase-shifted one-half p radians. A non-sinusoidal waveform is typically a periodic oscillation but is neither of these. Some examples are triangle waves, rectangle waves, square waves, trapezoid waves and saw tooth waves. Typically, they do not arise in nature, where inertia of rest and conservation of angular momentum preclude the abrupt transitions that characterize non-sinusoidal phenomena.

Non-sinusoidal waveforms are prominent in the world of electronics and they are readily synthesized. A non-sinusoidal waveform can be con- structed by adding two or more sine waves. The synthesis of a specific non-sinusoidal waveform is a matter of combining signals of the appro- priate frequency, amplitude and phase. In this manner square waves and similar non-linear waveforms can be constructed and represented graphically.

Such waveforms, known as complex waves, consist of one funda- mental frequency and one or more harmonic frequencies. By convention, the fundamental wave is the lowest frequency and generally the highest amplitude.



Q.8. (b) Write and explain two applications of differential amplifier with the help of its circuit diagrams.

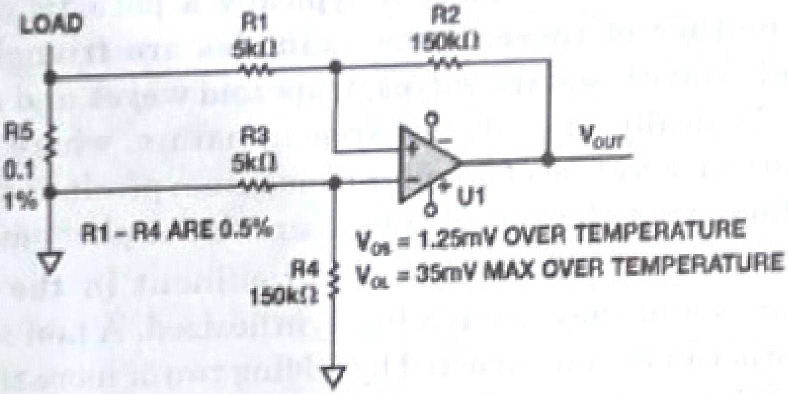
Ans. Ist application are:

The first suboptimal design is shown in Figure.

This design is a low-end current detection application using OP291. R1 to R4 are discrete 0.5% resistors. According to the formula in the article by Pallas-Areny, the optimal CMR is 64 dB.

Fortunately, the common-mode voltage is very close to the ground, so CMR is not the main source of error in this application. A current sense resistor with a tolerance of 1% will produce a 1% error, but the initial tolerance can be calibrated or adjusted.

However, since the operating range exceeds 80°C, the temperature coefficient of resistance must be considered.



For extremely low shunt resistance values, a 4-pin Kelvin sense resistor should be used. Using a high-precision 0.1 O resistor and directly con- necting the resistor with a PCB trace of a few tenths of an inch can easily increase 10 mO, resulting in an error of more than 10%. But the error will be greater because the temperature coefficient of the copper traces on the PCB exceeds 3000 ppm.

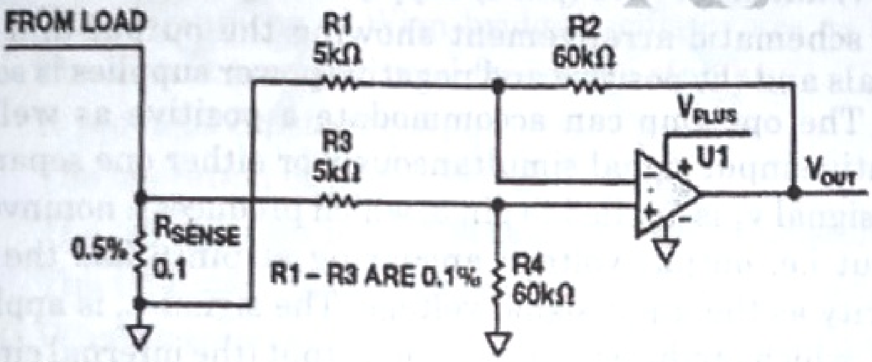
The shunt resistance value must be carefully selected. A higher value produces a larger signal. This is a good thing, but the power consumption -(I2R) will also increase, possibly up to several watts. With a smaller value (mO level), the parasitic resistance of the line and PCB trace may cause a larger error. Generally, Kelvin detection can be used to reduce these errors. We can use a special four-terminal resistor (such as Ohmite LVK series) or optimize the PCB layout to use standard resistors.

If the value is extremely small, PCB traces can be used, but this will not be very accurate.

2nd Application

This example has low noise gain, but it uses a low precision four-channel op amp with 3 mV offset, 10-μV/°C offset drift, and 79 dB CMR, And in the range of 0 A to 3.6 A, an accuracy of ±5 mA is required. If a ±0.5% detection resistor is used, the required ±0.14% accuracy cannot be achieved. If a 100 mO resistor is used, a ±5 mA current can produce a ±500 μV voltage drop.

Unfortunately, the offset voltage of an op amp with temperature is ten times greater than the measured value. Even if VOS is adjusted to zero, a temperature change of 50°C will exhaust the entire error budget. If the noise gain is 13, any change in VOS will be expanded by 13 times. To improve performance, zero-drift operational amplifiers (such as AD8638, ADA4051, or ADA4528), thin-film resistor arrays, and higher-precision sense resistors should be used.



Q.9. (a) Write the properties of ideal operational amplifier.

Ans. The op-amp is said to be ideal if it has the following characteristics:

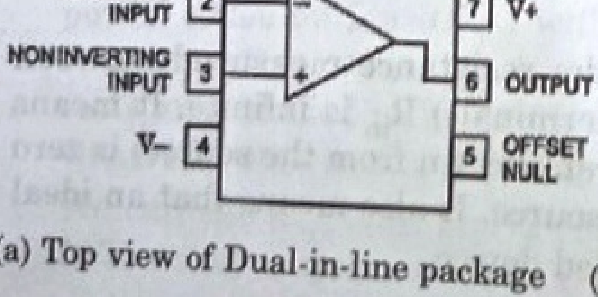
1. Its open-loop gain A is infinite. When an op-amp is operated without any connection between the output and any of the inputs (i.e., without feedback), it is said to be the open-loop condition. Infinite voltage gain means the voltage difference required between the two inputs to produce any output voltage is zero.
2. Its input resistance (i.e., the resistance measured between inverting and noniverting terminals) R_{in} is infinite. It means that the input current (current drawn from the source) is zero and so it does not load the source. It also means that an ideal op-amp is a voltage controlled device.

3. Its output impedance R_{out} is zero i.e., the output voltage v_{out} does not depend on the load resistance connected between the output terminal i.e., output voltage is independent of the current drawn by the load. The output thus can be drive an infinite number of other devices.
4. Perfect balance. Because of infinite voltage gain, the voltage between the inverting and noninverting terminal of input i.e., differential input voltage $v_d = v_2 - v_1$ is essentially zero (i.e., $v_1 = v_2$) for finite terminals of input i.e., differential input voltage $v_d = v_2 - v_1$ is essentially zero (i.e., $v_1 = v_2$) for finite output voltage v_{out}. This implies that v_1 and v_2 track each other i.e., a virtual short circuit exists between the two input terminals but with no current flowing between the two terminals, as R_{in} is infinite.

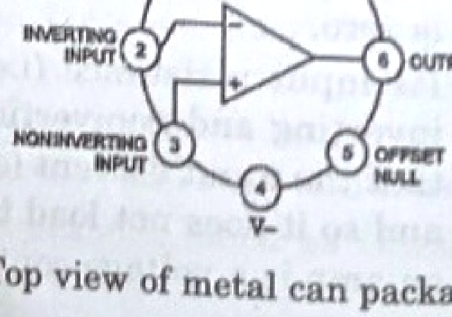
Q.9. (b) Draw the pin configuration of 741 op-amp IC and explain its working.

Ans. Fig. (a) shows the connection terminals for a signal 741 op-amp in a dual-in-line package and **Fig. (b)** shows the connection termi- nals for a 741 enclosed in a metal can package. From Fig. (a) and (b) it is obvious that there are two input terminals (pins 2 and 3) and one output terminal (pin 6). Both a positive (pin 7) and nega- tive (pin 4) supply voltage must be furnished. The schematic arrangement showing the output and input signals and the positive and negative power supplies is sown in Fgi. The op- amp can accommodate a positive as well as a negative input signal simultaneously or either one separately. The signal v_1 is applied to pin 3, which produces a noninverting output i.e. output voltage appearing at pin 6 has the same polarity as the input signal voltage. The signal v_2 is applied to pin 2, which produces an inverting output (the internal circuitry of the op-amp yields an output signal of inverted or opposite polarity). The design of the op-amp is such that the output voltage is related to the two input voltage by equation

$$v_{out} = A(v_1 - v_2) = Av_d$$



(a) Top view of Dual-in-line package



(b) Top view of metal can package

2020

Basic Electronics

Q.1. Fill in the Blanks/answer any seven of the following:

(a) In CB configuration, output characteristics may be shown by plot of .....

Ans. I w.r.t V_{CB}

(b) The........ carriers enter the channel region through the ..... terminal and leave the channel through the............... terminal in JFET.

Ans. Minority, gate, drain

(c) Mention the advantages of Wien bridge oscillator.

Ans. The advantages of Wien bridge oscillator are as follows -
The circuit provides good frequency stability.
It provides constant output.
The operation of circuit is quite easy.
The overall gain is high because of two transistors.
The frequency of oscillations can be changed easily.

(d) What is reverse leakage current in CE configuration?

Ans. The term "$(\beta+1)I_{CBO}$" is the reverse leakage current in common emitter configuration. It is denoted by I_{CEO}. Since β is much greater than I, $I_{CEO} > I_{CBO}$ The leakage current in common emitter configuration is larger than that of common base configuration.

(e) How is amplifier different from the oscillator?

Ans. The crucial factor which differentiates amplifier and oscillator is its usage. The amplifier is used as a multiplier circuit which is used for increasing the intensity of weak signal while the oscillator is used as a source in an electronic circuit. The main use of oscillator is for wave- form generation.

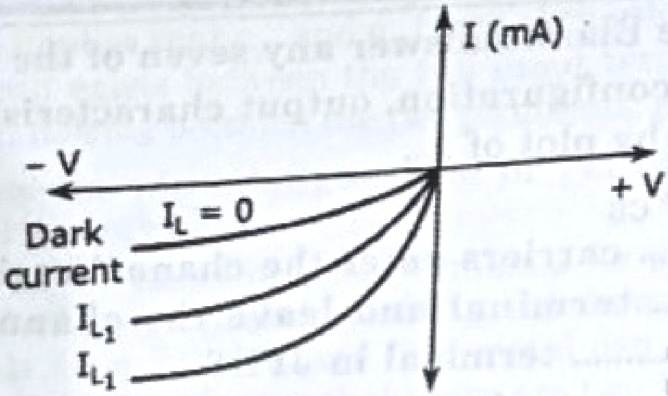
(f) Name the breakdown mechanism in the lightly doped

P-N junction diode under reverse biased condition.

Ans. p-n junction is an active element of the circuit, which is used where we want the flow of current in one direction and not in both. It is called a p- n junction because it is built using a p-type and a n-type semiconductor. When this diode is forward biased, only in that case it allows the current.

(g) Draw the V-I characteristics of photodiode.

Ans.



(b) IV characteristic

(h) What is transconductance with reference to JFET?

Ans. The transconductance cruve of a JFET transistor is the the graph of the drain current, ID verses the gate-source voltage, VGS. The ratio of change in drain current, ΔID, to the change in gate-source voltage, ΔVGS, is the transconductance, gm. The unit of transconductance is the siemen (S). It is the reciprocal of resistance (Ω).

(i) What is the effect of removing bypass capacitor across the emitter resistor in case of CE amplifier ?

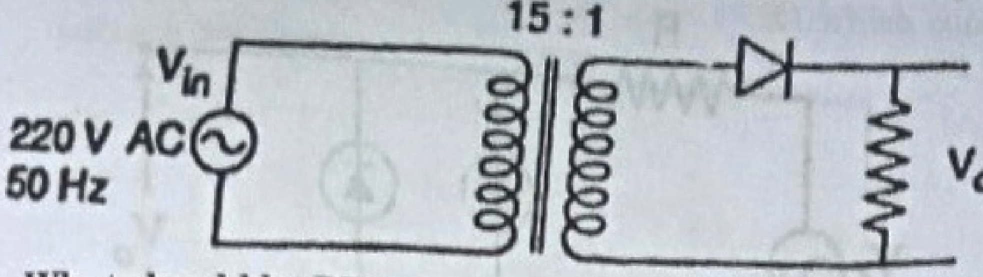
Ans. Whenever bypass capacitor is connected in parallel with an emitter resistance, the voltage gain of CE amplifier increases. If the bypass capacitor is removed, an extreme degeneration is produced in the amplifier circuit and the voltage gained will be reduced.

(j) What is meant by phase reversal ?

Ans. A phase reversal fault is a situation where two phases in a three phase system have been swapped. This typically occurs during equipment in- stallation, upgrades or general maintenance. 3-phase motors and other rotating equipment rely on the order of the phases to be correct.

Q.2. (a) Find the DC voltage, ripple factor and efficiency for

the half- wave rectifier given in the circuit below:



What should be PIV of the diode used? If bridge rectifier is used for same power supply, what will be the value of DC voltage and PIV of diode ?

Ans. $V_i = V_m \sin \omega t$

$V_m = 220V$

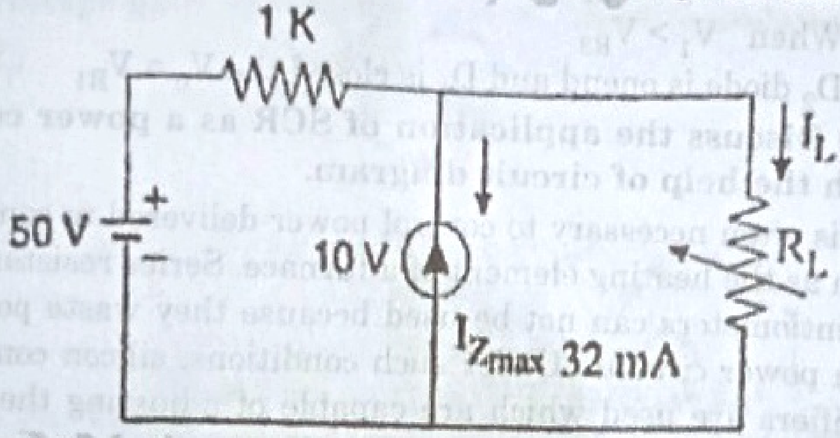
$f = 50$ Hz

Peak voltage = 220/15 – 0.7 = 14 volt

DC voltage = 14 × 7/22 = 4.45 volt

Bridge rectifier = 2 × DC voltage = 2 × 4.45 = 8.9 volt

(b) Calculate the range of I, and R, so that VRL being maintained at 10V and also calculate the value of maximum voltage rating in the circuit given below:



Ans. VRL = 10 volt

voltage = 50 volt

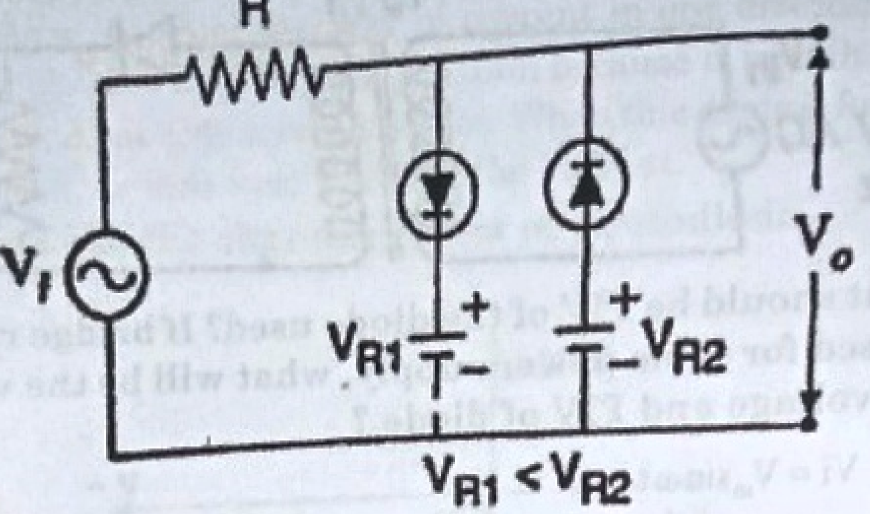
$I_{zmax} = 32mA, \; I_{zmin} = 0A$

$$I_S = \frac{50-10}{1\times10^3} = 40\,mA$$

When I_Z is minimum then $R_{L1} = 10/40 \times 10^3 = 250\ \Omega$

Q.3(a) Draw the waveform of output V, and explain the

operation of circuit given below:



Ans. $V_{R1} < V_{R2}$

(i) When $V_i < V_{R1}$

Diode D_1 is open and D_2 is closed

$$V_0 = V_{R2}$$

(ii) When $V_{R1} < V_{R2}$

Both diode D_1 and D_2 are closed then both the DC Batteries are parallel

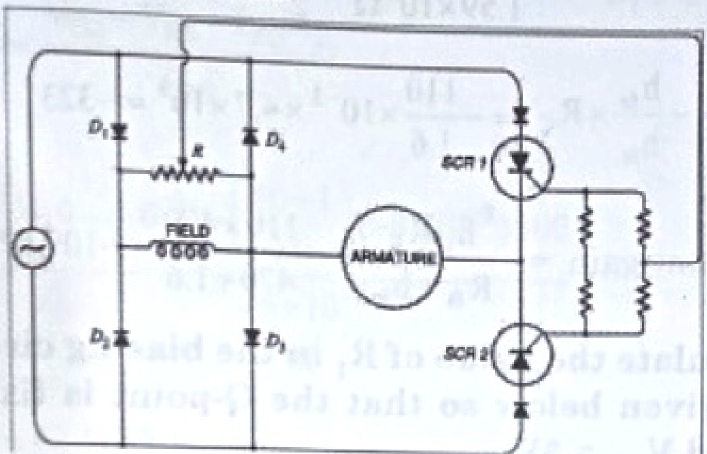
$$V_0 = V_{R2}$$

(iii) When $V_1 > V_{R2}$

D_2 diode is opend and D_1 is closed the $V_0 = V_{R1}$

Q.3. (b) Discuss the application of SCR as a power control with the help of circuit diagram.

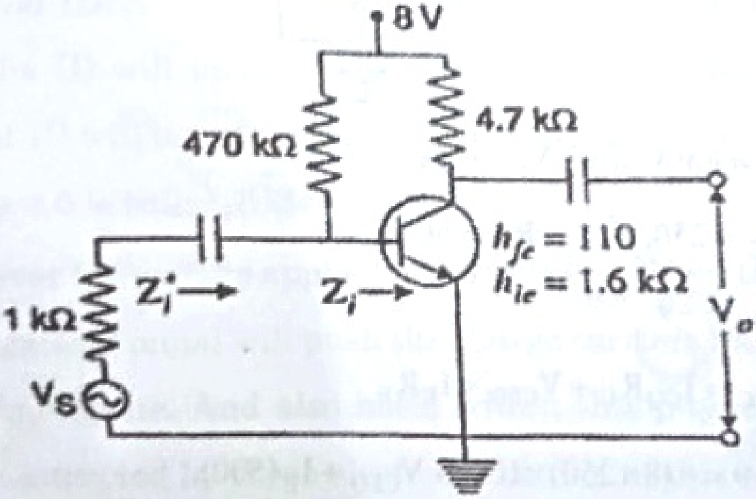
Ans. It is often necessary to control power delivered to some load such as the heating element of a furnace. Series resistances or potentiometers can not be used because they waste power in high power circuits. Under such conditions, silicon controlled rectifiers are used which are capable of adjusting the transmitted power with little waste. Fig. shows a common circuit for controlling power in the load R_L. During the positive half-cycle of a.c. supply, end A is positive and end B is negative. Therefore, capacitor C_2 is charged through $AD_1RC_2\ D_4B$. The charge on the capacitor C_2 depends upon the value of potentiometer R. When the capacitor C_2 is charged hrough a sufficient voltage, it discharges through the zener Z. This gives a pulse to the primary and hence secondary of transformer T_2. This turns on SCR2 which conducts currents through the load R_L. During negative half-cycle of supply, the capacitor C_1 is charged. It discharges through the zener and fires SCR1 which conducts current through the load.



The angle of conduction can be controlled by the potentiometer R The greater the resistance of R, lesser is the voltage across C_1 or C_2 and hence smaller will be the time during which SCRI and SCR2 will conduct in a full cycle. In this way, we can control a large power of several kW in the load R_L with the help of a small potentiometer R.

Q.4(a) For the network given below, determine the following parameter using the approximate equivalent model.

Voltage gain A_v, current gain A, input impedance Z_i' and Z_i:



Ans. $h_{fe} = 110 R_B = 470k\Omega$

$h_{ie} = 1.6k\Omega$ $R_C = 4.7k\Omega$

$R_J = 1k\Omega$

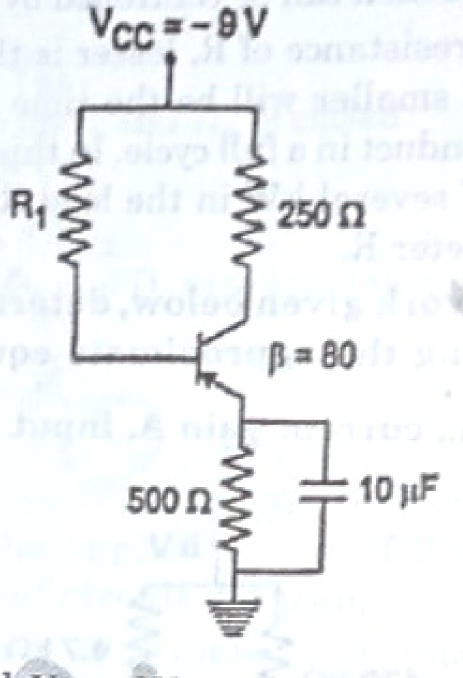
(i) $z_i = R_B \times h_{ie} = 470\times10^3 \times 1.6\times10^3$

$$1.59\times10^3\Omega$$

(ii) $A_V = -\frac{h_{fe}}{h_{ie}}\times R_C = -\frac{110}{1.6}\times10^{-3}\times4.7\times10^3 = -323$

(iii) Current gain $= -\frac{h_{fe}R_B}{R_B+h_{ie}} = -\frac{110\times470}{470+1.6} = -109.62$

Q.4(b) Calculate the value of R_1 in the biasing circuit in the figure given below so that the Q-point is fixed at I_C = 8mA and V_{CE} = 3V.



Ans. $I_C = 8mA$ and $V_{CE} = 3V$

$R_C = 250;$ $R_E = 500$

$V_{CC} = -9$

$V_{CC} = I_{CQ}R_C + V_{CEQ} + I_ER_E$

$-9 = -(8\times250)\times10^{-3} + V_{CEQ} + I_E(500)$

$$I_E = \frac{(\beta+1)I_C}{\beta}$$

$$I_E = \frac{81}{80} \times 8 \times 10^{-3}$$

$$RB = \frac{V_{CC} - V_{BE} - I_{EQ}R_E}{I_{BQ}}$$

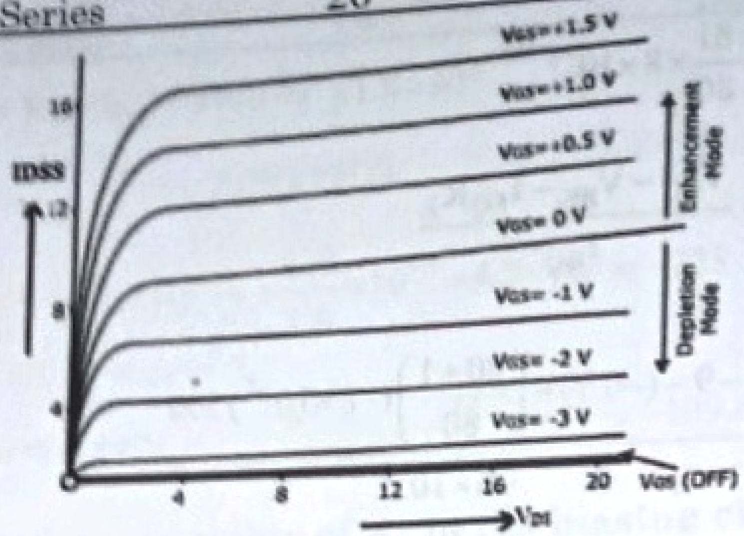
$$= \frac{-9-(-0.7)-\left(\frac{80+1}{80}\right)(-8\times10^{-3})500}{\frac{-8\times10^{-3}}{80}}$$

$$= 42.5K\Omega$$

Q.5. (a) Given a deletion-type MOSFET. In the positive V_{GS} region, does the drain current increase at a significantly higher rate than for negative value? Does the I_D curve become more and more vertical with increasing positive values of V_{GS} ?

Ans. The drain characteristics of the n channel depletion MOSFET are shown below. These characteristics are plotted between the VDS and IDSS. When we keep on increasing the VDS value then the ID will increase. After a certain voltage, the drain current ID will become constant. The saturation current value for Vgs = 0 is called IDSs.

Whenever the voltage applied is negative, and then this voltage at the gate terminal will push the charge carriers like electrons to the substrate. And also holes within this p-type substrate will be attracted by these electrons. So due to this voltage, the electrons within the channel will be recombined with holes. The rate of the recombination will depend on the negative voltage applied.



Drain Characteristics of N channel MOSFET

Once we increase this negative voltage, the recombination rate will also increase so which will decrease the no. of electrons available within this channel and will reduce the current flow effectively.

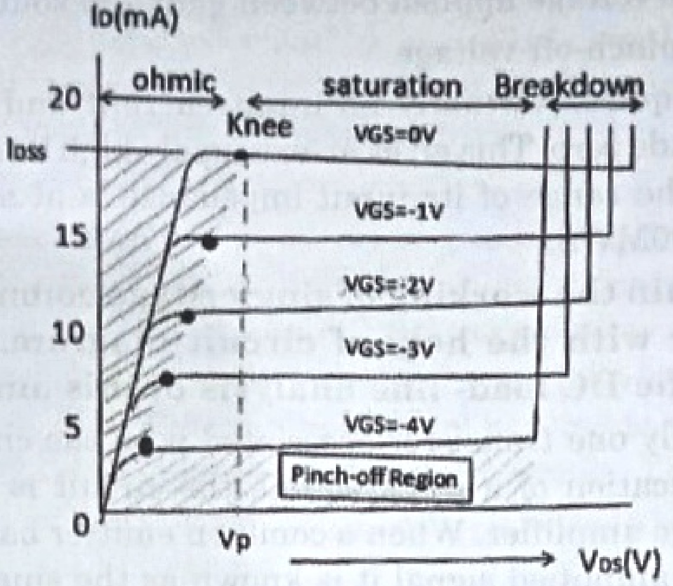
When we observe the above characteristics, it is seen that when the VGS value will becomes more negative then the drain current will decreases. At a certain voltage, this negative voltage will become zero. This voltage is known as pinch-off voltage.

This MOSFET also works for the positive voltage, so when we apply the positive voltage at the gate terminal then the electrons will be attracted to N- channel. So the no. of electrons within this channel will increase. So the current flow within this channel will increase. So for the positive Vgs value, the ID will be even more than IDSS.

Q. 5. (b) Draw V-I characteristics curves of JFET and mark various re- gions. Explain how FET is voltage-controlled device.

Ans. The V-I characteristics of N-channel JFET are shown below. In this N-channel JFET structure the gate voltage (VGs) controls the current flow between the source drain. The JFET is a voltage controlled device so no current flows through the gate, then the source current (I_S) is equal to the drain current (I_D) i.e. ID = I_S.

In this V-I characteristic the voltage VGs represents the voltage applied between the gate and the source and the voltage VD_S represents the voltage applied between the drain and source.



The JFET has different characteristics at different stages of operation depending on the input voltages and the characteristics of JFET at different regions

1. **Ohmic Region:** If $VG_S = 0$ then the depletion region of the channel is very small and in this region the JFET acts as a voltage controlled resistor.
2. **Pinched-off Region:** This is also called as cut-off region. The JFET enters into this region when the gate voltage is large negative, then the channel closes i.e.no current flows through the channel.
3. **Saturation or Active Region:** In this region the channel acts as a good conductor which is controlled by the gate voltage (VG_S).
4. **Breakdown Region:** If the drain to source voltage (VD_S) is high enough, then the channel of the JFET breaks down and in this region uncontrolled maximum current passes through the device.

FET is called a voltage-controlled device. In the case of a FET the output current ID is a function of the voltage VG_S applied to the input circuit. Hence FET is known as a voltage controlled device. The equation that governs the working of a FET is called Shockley's equation given by,

$ID = IDS_S\,[1-(VG_S/V_P)\,2$

where, ID is the drain current

Ipss is the maximum saturation current

VG_S is the voltage applied between gate and source

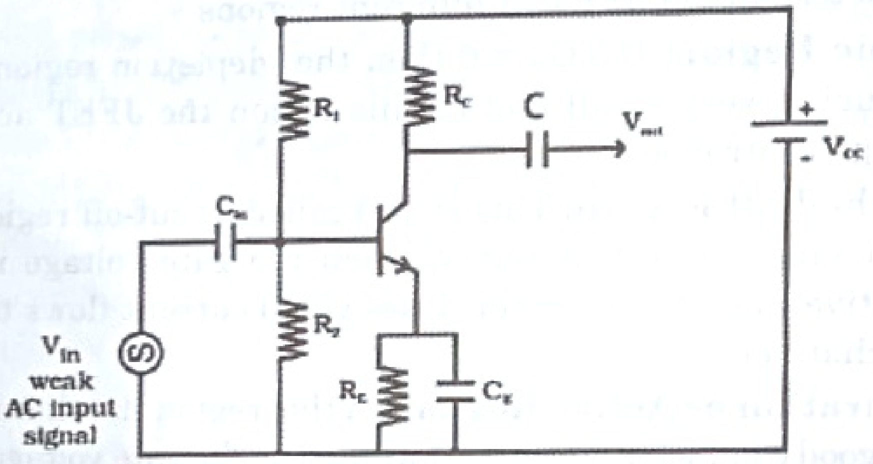
V_P is the pinch-off voltage

A FET requires virtually no input current and hence IG is always made zero. This gives an extremely high input resistance to FET. The range of its input impedance is at a level of I to several 100MWS.

Q.6. (a) Explain the working of single-stage common emitter amplifier with the help of circuit diagram. Draw and explain the DC load- line analysis of this amplifier.

Ans. When only one transistor associated with the circuit is used for amplification of a weak signal, the circuit is known as a single-stage amplifier. When a common emitter base is used to collect the amplified signal it is known as the single stage CE amplifier.

The diagram of a single stage CE amplifier is given below



A simple stage CE amplifier has different circuit elements and functions. Let us discuss about that,

The resistance R_1, R_2, R_E shown in the diagram forms the biasing circuit.

The circuit used to couple the signal to the base of the transistor is known as the input capacitance, Cin circuit. The signal source resistance will come across R_2 if this circuit is not used, and thus change the bias. The capacitor C_{in} allows only a.c. signal to flow through it.

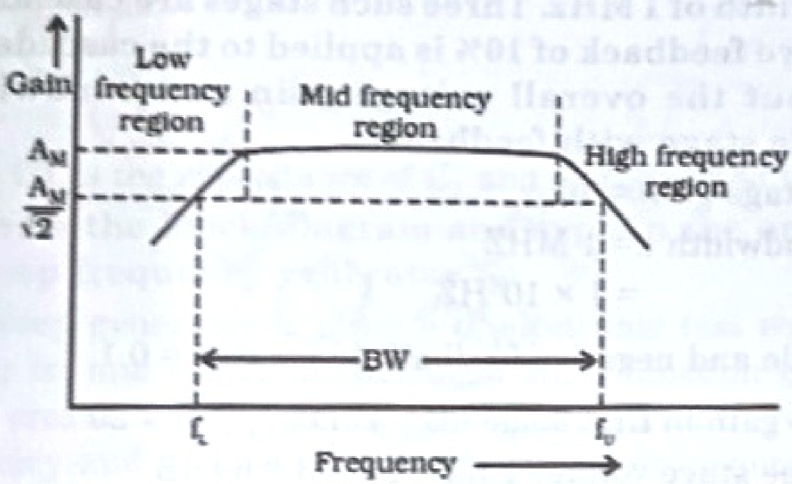
The capacitor connected in parallel with R_E to provide a low reactance path to the amplified AC signal is known as the

Emitter bypass capacitor CE. If this capacitor is not used, then the amplified AC signal flowing through R_E will cause a voltage drop across it, thereby shifting the output voltage.

The capacitor used to couple the amplified signal to the output device is known as coupling capacitor C. This capacitor C allows only a.c. signal to flow through it.

Working :

A small base current flows when a weak input a.c. signal is given to the base of the transistor. A much larger a.c. current flows through collector load RC due to transistor action. A large voltage appears across RC and hence we get a large voltage at the output. Therefore, a weak signal applied to the base came out in amplified form in the collector circuit. The ratio of the amplified output voltage to the input voltage in the amplifier is known as the Voltage gain (Av) of the amplifier.



The above diagram shows the frequency response curve

The voltage gain (Av) of the amplifier for different input frequencies can be determined using the frequency response graph. Taking frequency (f) along X-axis and voltage gain (Av) along Y-axis a graph is drawn. The frequency response curve obtained from the graph it will be like the one which is shown in the diagram above

It is seen that the amplifier gain decreases at very low frequency and at very high frequency, but over a wide range of mid frequency regions it remains constant. The frequency in the low frequency range at which the gain of the amplifier is 12 – $\sqrt{\ }$ times the mid frequency gain (AM) is known as the lower cut off frequency.

The frequency in the high frequency range at which the gain of the amplifier is $12-\sqrt{\ }$ times the mid frequency gain (AM) is known as the upper cut of frequency.

The frequency interval between lower cut off and upper cutoff frequencies is known as the Bandwidth of the single stage CE amplifier.

$$BW = (f)_u - (f)_l$$

Where,

BW is the bandwidth

(f)u: is the upper cut of frequency.

(f)l: is the lower cut off frequency.

Q.6. (b) A single-stage amplifier has voltage gain of 10 and bandwidth of 1 MHz. Three such stages are cascaded and negative feedback of 10% is applied to the cascade stage. Find out the overall voltage gain and bandwidth of cascade stage with feedback.

Ans. Voltage gain = 10

Bandwidth : = 1 MHZ

$= 1 \times 10^6$ HZ

Casecade and negative feedback (β) = 10% = 0.1

Voltage gain in first stage dB = 20Log_{10} (10) = 20

For three stage voltage gain = 20 × 3 = 60 dB

$f_0 = 1 \times 10^6$ HZ

Bandwidth with cascade is

$f' = (1+A_0\beta)\, f_0 = 7 \times 1 \times 106$ Hz = 7 MHz

Q.7.(a) Explain the operation of Colpitts oscillator with the help of circuit diagram.

Ans. The emitter terminal of the transistor is effectively connected to the junction of the two capacitors, C_1 and C_2 which are connected in series and act as a simple voltage divider. When the power supply is firstly applied, capacitors C_1 and C_2 charge up and then discharge through the coil L. The oscillations across the capacitors are applied to the base-emitter junction and appear in the amplified at the collector output.

Resistors, R_1 and R_2 provide the usual stabilizing DC bias for the transistor in the normal manner while the additional capacitors act as a DC blocking bypass capacitors. A radio-frequency choke (RFC) is used in the collector circuit to provide a high reactance (ideally open circuit) at the frequency of oscillation, (*fr*) and a low resistance at DC to help start the oscillations. The required external phase shift is obtained in a similar manner to that in the Hartley oscillator circuit with the required positive feedback obtained for sus- tained undamped oscillations. The amount of feedback is determined by the ratio of C_1 and C_2. These two capacitances are generally "ganged" together to provide a constant amount of feedback so that as one is adjusted the other automatically follows.

The frequency of oscillations for a Colpitts oscillator is determined by the resonant frequency of the LC tank circuit and is given as:

$$f_r = \frac{1}{2\pi\sqrt{LC_T}}$$

where CT is the capacitance of C_1 and C_2 connected in series.

Q.7.(b) Draw the block diagram and explain the operation of sweep frequency generator ?

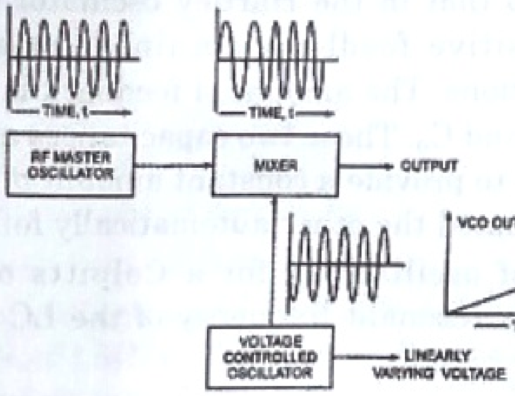
Ans. A sweep generator is a piece of electronic test equipment similar to, and sometimes included on, a function generator which creates an electrical waveform with a linearly varying frequency and a constant amplitude. Sweep generators are commonly used to test the frequency response of electronic filter circuits. These circuits are mostly transistor circuits with inductors and capacitors to create linear characteristics.

Sweeps are a popular method in the field of audio measurement to describe the change in a measured output value over a progressing input parameter. The most commonly-used progressive input parameter is frequency varied over the standard audio bandwidth of 20 Hz to 20 kHz.

A sweep frequency generator or sweeper is a special type of signal generator in which the output frequency is cyclically swept through a range of frequencies.

The instruments may have a display built into it to show the variation of amplitude with frequency or it may provide signals for use with an external oscilloscope. Shows the block diagram of typical sweep generator.

The time base is usually adjustable to give output sweep times in the range from 10 ms to greater than 100s. it is also often possible to control the sweep manually from the front panel of the instrument. The time base is frequently a triangular or a sawtooth waveform.



The block diagram of an electronically tuned sweep frequency generator is shown in the figure below. The most important component of a sweep-frequency generator is the master oscillator. It is mostly an RF type and has many Operating ranges which are selected by a range switch

Two modes are used to set the swept frequency range:

(i) The stop-start Mode: in this mode the stop and start frequencies are set from the front panel and the instrument sweeps between these limits. This mode is used for wide sweep widths.

(ii) Delta Frequency Mode: in this mode the centre frequency and the maximum excursion about this frequency are set from the front panel. It is used for narrow sweep widths. The frequency range of the swept frequency generator usually extends over the three bands, 0.001 Hz to 100 kHz (low frequency to audio), 100 kHz to 1500 MHz (RF RANGE) and 1200 GHz (microwave range). Three ap- proaches may be used to cover a wide band of swept frequencies from a single instrument.

(a) Manually Switching: Between different frequency oscillators, the problem occurs when the frequency range needed overlaps two bands.

(b) Stacked Switching: The bands are automatically selected by electronic switches so that one can sweep the whole instruments range as one continuous band.

(c) Heterodyne control: Illustrated in given. Two high frequency signals are mixed to give a lower difference frequency O/P as one continuous band.

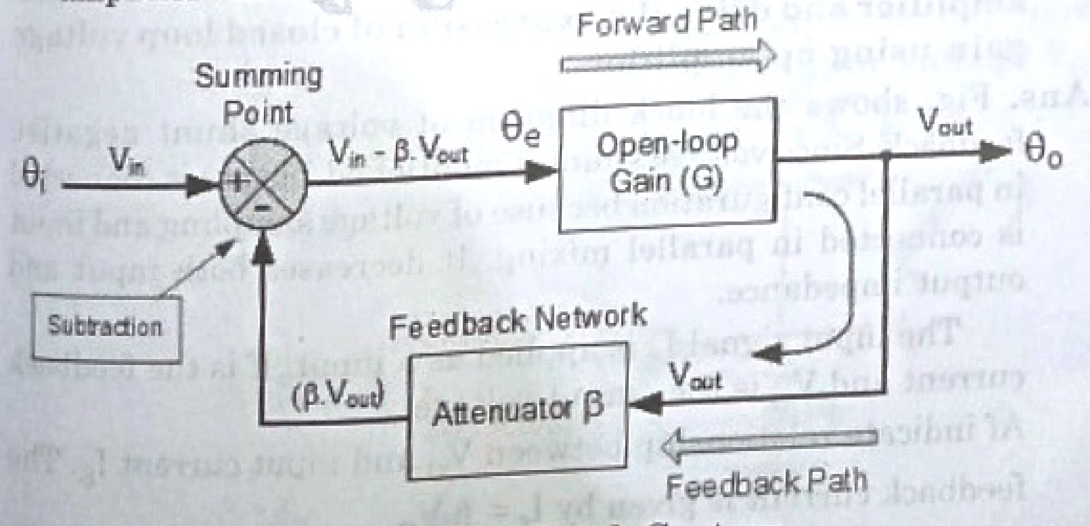
Output level control is used in swept frequency generator to keep the output amplitude to the values set on the front dial. Usually RF amplitude of CS the output. This is compared with a signal corresponding to the required amplitude and the error is fed back to an electronic attenuator circuit to keep the output constant.

Q.8. (a) Discuss with the help of circuit diagram the purpose of providing negative feedback and positive feedback.

Ans. Negative Feedback Systems : In a "negative feedback control system", the set point and output values are subtracted from each other as the feedback is "out-of-phase" with the original input. The effect of negative (or degenerative) feedback is to "reduce" the gain. For example, if someone criticises you or gives you negative feedback about something, you feel unhappy about yourself and therefore lack energy, you feel less positive.

Because negative feedback produces stable circuit responses, improves stability and increases the operating bandwidth of a given system, the majority of all control and feedback systems is degenerative reducing the effects of the gain.

An example of a negative feedback system is an electronic amplifier based on an operational amplifier as shown.



Positive Feedback System

Positive feedback control of the op-amp is achieved by applying a small part of the output voltage signal at Vout back to the non-inverting (+) input terminal via the feedback resistor, Rf.

If the input voltage Vin is positive, the op-amp amplifies this positive signal and the output becomes more positive. Some of this output voltage is returned back to the input by the feedback network.

Thus the input voltage becomes more positive, causing an even larger output voltage and so on. Eventually the output becomes saturated at its positive supply rail.

If the input voltage V_{in} is negative, the reverse happens and the op-amp saturates at its negative supply rail. Then we can see that positive feedback does not allow the circuit to function as an amplifier as the output voltage quickly saturates to one supply rail or the other, because with positive feedback loops "more leads to more" and "less leads to less".

Then if the loop gain is positive for any system the transfer function will be: Av = G / (1 – GH). Note that if GH = 1 the system gain Av = infinity and the circuit will start to self-oscillate, after which no input signal is needed to maintain oscillations, which is useful if you want to make an oscillator.

We have seen that positive or regenerative feedback increases the gain and the possibility of instability in a system which may lead to self-oscillation and as such, positive feedback is widely used in oscillatory circuits such as Oscillators and Timing circuits.

Q. 8. (b) Draw the circuit diagram of voltage shunt feedback amplifier and drive the expression of closed loop voltage gain using op-amplifier.

Ans. Fig. shows the block diagram of voltage shunt negative feedback. Since voltage shunt is mentioned, output is connected in parallel configuration because of voltage sampling and input is connected in parallel mixing. It decreases both input and output impedance.

The input signal I_S is applied as a input, If is the feedback current and V_O is the output voltage.

Af indicate relationship between V_O and input current I_S. The feedback current is given by $I_f = \beta V_O$.

Resistance amplifier is called so because output is voltage and input is current, hence ratio gives us resistance gain.

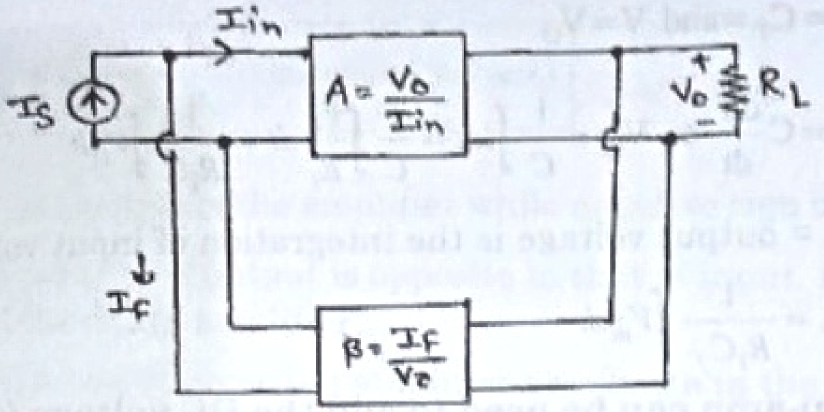


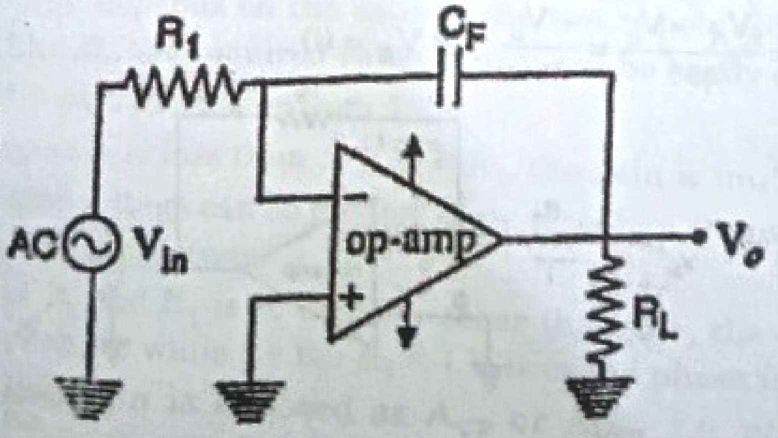
Fig. 1: Block diagram of Voltage Shunt Negative Feedback

The sample of output voltage is applied as a input to feedback network which feeds back the output signal to the input.

The difference of input signal and feedback signal gets amplified by the resistance amplifier.

- The closed loop mode of op-amp is possible using feedback. The feedback allows to feed some part of the output back to the input. The feedback helps to control gain which otherwise drives op-amp into saturation.
- The negative feedback is possible by adding a resistor as shown in the Fig. called feedback resistor.
- The feedback is said to be negative as the feedback resistor connects the output to the inverting input terminal.
- The gain resulting with feedback is called closed loop gain of the op-amp.

Q.9(a) Explain the operation performed by the circuit given below and derive the expression of output voltage V_O.



Ans. $Q = CV$ and $\frac{dq}{dt} = C\frac{dV}{dt}$

$C = C_f$ =and $V = V_O$

$$i = C\frac{dV}{dt} \text{ or } V_O = -\frac{1}{C}\int i dt = -\frac{1}{C}\int \frac{V_i}{R_i} dt = -\frac{1}{R_1 C}\int V_i dt$$

V_0 = output voltage is the integration of input voltage Vi

$$V_o = -\frac{1}{R_1 C_f}\int V_{in} dt$$

Q.9. (b) Op-amp can be used to add the DC voltage (addition operation). Draw the circuit and explain the operation of adder using op-amp non inverting mode.

Ans. An amplifier which provides a phase shift of 180° between input and output is called inverting amplifier.

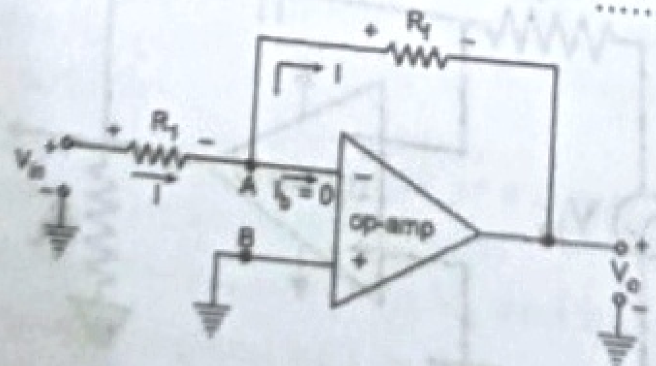
- The basic circuit diagram of an inverting amplifier using op-amp is shown in the Fig. (a).
- By the concept of virtual ground the two input terminals are always at the same potential.
- As node B is grounded, node A is also at ground potential, from the concept of virtual ground,

so $V_A = 0$

$$\therefore \quad I = \frac{V_{in} - V_A}{R_1} = \frac{V_{in}}{R_1} \quad (\text{as } V_A = 0) \qquad \text{..........(1)}$$

- The op-amp input current is always zero hence entire current I passes through the resistance R_f.
- Now from the output side, considering the direction of current I we can write,

$$I = \frac{V_A - V_o}{R_f} = \frac{-V_o}{R_f} \quad (\text{as } V_A = 0) \qquad \text{..........(2)}$$



(a) Inverting amplif...

- Equating (1) and (2) we get, $\frac{V_{in}}{R_1} = -\frac{V_o}{R_f}$

$$\therefore \quad \boxed{A_V = \frac{V_o}{V_{in}} = -\frac{R_f}{R_1} \text{(Gain with feedback)}} \quad \text{...........(3)}$$

- The $\frac{R_f}{R_1}$ is the gain of the amplifier while negative sign indicates that the polarity of output is opposite to that of input. Hence it is called inverting amplifier.
- The waveforms of inverting amplifier are shown in the Fig. (b).

- The $\frac{R_f}{R_1}$ is the gain of the amplifier while negative sign indicates that the polarity of output is opposite to that of input. Hence it is called inverting amplifier.
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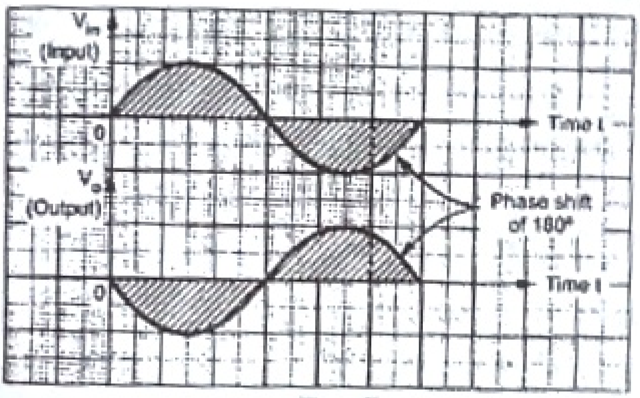

Observations :

1. The output is inverted with respect to input, which is indicated by minus sign.
2. The voltage gain is independent of open loop gain of the op-amp, which is assumed to be large.
3. The voltage gain depends on the ratio of the two resistances. Hence selecting R, and R,, the required value of gain can be easily obtained.
4. If $R_f > R_1$, the gain is greater than 1.
   If $R_f < R_1$, the gain is less than 1. If $R_f = R_1$, the gain is unity.
   Thus the output voltage can be greater than, less than or equal to the input voltage, in magnitude.
5. If the ratio of R_f and R_1 is K which is other than one, the circuit is called scale changer while for $R_f / R_1 = 1$ it is called phase inverter.
6. The closed loop gain is denoted as A_{VF} or A_{VCL} i.e. gain with feedback.

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2021

BASIC ELECTRONICS

1. Answer the following questions (any seven):

(a) Derive the relation between β and α of a transistor. What is reverse leakage current in CE configuration?

Ans: $\alpha = \Delta I_C \ / \ \Delta I_E$

$\beta = \Delta I_C / \Delta I_B = \Delta I_C / \Delta I_E \times \Delta I_E / \Delta I_B = \alpha \times \Delta I_E / \Delta I_B$ ....(1)

$\Delta I_B = \Delta I_E - \Delta I_C$ ....(2)

Substituting the equation (2) in equation (1) we get,

Substituting the equation (2) in equation (1) we get,

$$\beta = \alpha \times \frac{\Delta I_E}{\Delta I_E - \Delta I_C}$$

$$\beta = \alpha \times \frac{1}{1 - \frac{\Delta I_C}{\Delta I_E}}$$

we know $\alpha = \Delta I_C \ / \ \Delta I_E$ therefore we get,

$$\beta = \frac{\alpha}{1-\alpha}$$

The reverse leakage current in common emitter configuration is denoted by I_{CEO}. The leakage current in common emitter configuration is larger than that of common base configuration.

(b) What is modulation index in AM?

Ans: Modulation index is also known as modulation depth is defined for the carrier wave to describe the modulated variable of the carrier signal varying with respect to its unmodulated level. It is represented as follows:

$$\mu = \frac{A_m}{A_C}$$

(c) What is the concept of frequency reuse in cellular network?

Ans: Frequency Reuse is the scheme in which allocation and reuse of channels throughout a coverage region is done. Each cellular base station is allocated a group of radio channels or Frequency sub-bands to be used within a small geographic area known as a cell. The shape of the cell is Hexagonal. The process of selecting and allocating the frequency sub-bands for all of the cellular base station within a system is called Frequency reuse or Frequency Planning.

(d) What is the use of offset null input in the operational amplifier? How are they used?

Ans: The op amp offset null capability is used to null any small DC offsets at the output for DC amplifiers. The offset null connections present on many operational amplifiers chips can be used to null any small DC offsets that might appear if the capability were not used.

(e) Why is negative feedback desired in amplifier application?

Ans: The applied negative feedback can improve its performance (gain stability, linearity, frequency response, step response) and reduces sensitivity to parameter variations due to manufacturing or environment.

(f) Emitter bias or sell-bias is more stable than fixed bias. Justify.

Ans: As temperature increases, I_c increases and internal resistance of the transistor decreases. It leads to the shifting of operating point and thus the circuit loses its stability. To overcome it we can add a swamping resistor in the emitter end of the circuit which increases the voltage at the emitter end with the increase of I_c with respect to temperature. This voltage opposes forward bias and reduces I_B and I_C. In fixed bias circuit this resistor is not present but in self-bias circuit this resistor is present. So self-bias circuit is more stable than fixed bias circuit against the variation in temperature.

(g) Explain how the process of avalanche breakdown occurs in a P-N junction diode. How is it different from Zener breakdown?

Ans: The main difference between Zener breakdown and avalanche breakdown is their mechanism of occurrence. Zener breakdown occurs because of the high electric field. The avalanche breakdown occurs because of the collision of free electrons with atoms.

(h) Justify that $\bar{m}_j = M_j$, where m_j and M_j are jth minterm (product term) and maxterm (sum term) respectively.

Ans: let's take an example $m_j = ABC$

according to demorgan's theorem.

$\bar{m}_J = \overline{ABC} = \bar{A} + \bar{B} + \bar{C} = M_j$

We can say that minterm and maxterm are compliment if each other and follow demorgan's theorem.

(i) Mention the disadvantages of Wien bridge oscillator.

Ans: The disadvantages of the Wien bridge oscillator are as follows:

- It can cause high output distortion.
- It cannot generate high frequencies.
- It has high number of components due to the two transistors.

(j) Which BJT amplifier ?

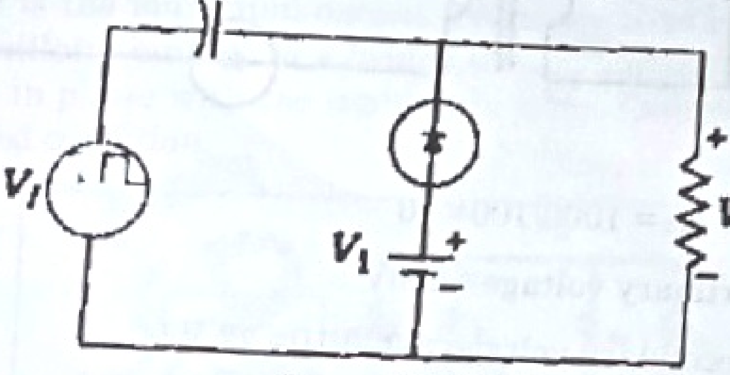
Ans. There are three basic BJT amplifier configurations that are generally identified as: common- emitter, common-base, and common-collector (sometimes called the emitter-follower). Each of these configurations exhibit certain characteristics that make them more desirable in certain circuit applications than the others.

(h) Justify that $\bar{m}_j = M_j$, where m_j and M_j are jth minterm (product term) and maxterm (sum term) respectively.

Ans: Application of one shot multivibrator

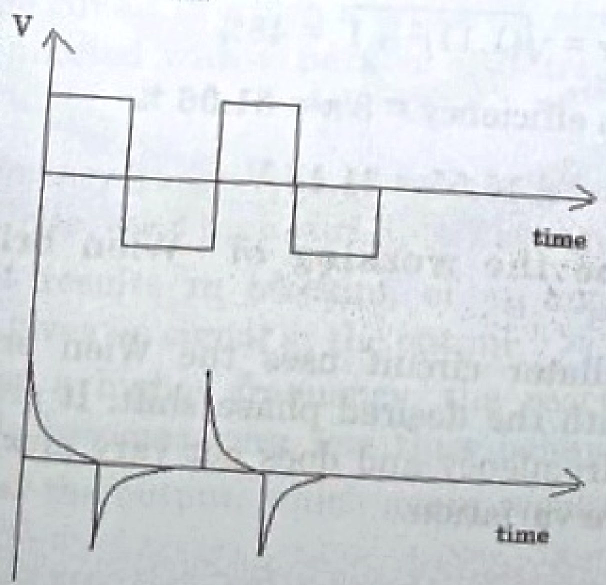
- A one shot multivibrator is basically used in the regeneration of a distorted pulse. It provides a sharp pulse from a distorted pulse.
- The output of the one shot multivibrator is used to trigger any other pulse generator circuit.

2.(a) Draw flit waveform of output voltage V_0 if input is square wave and explain the operation of circuit given below :

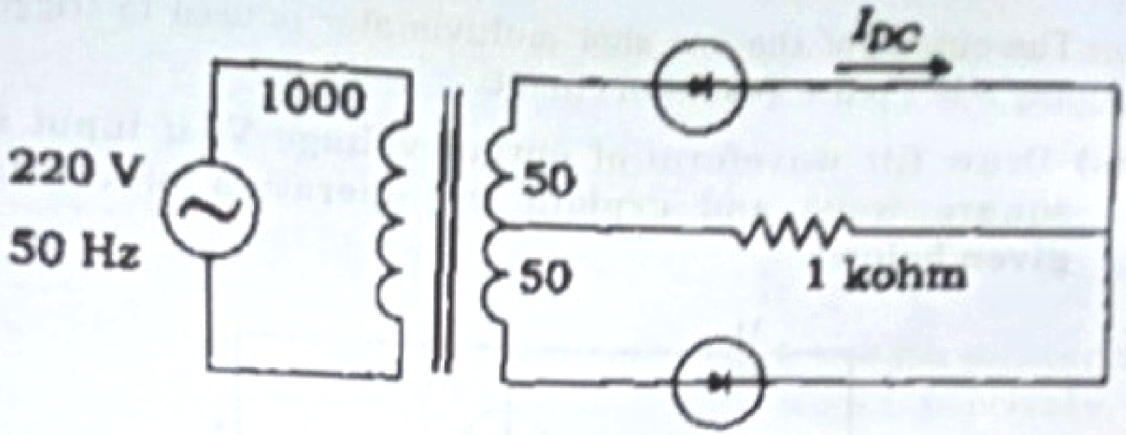


Ans. Diode is in forward bias, So it will behave as close switch. When square wave is passed through the capacitor is gives triangular waveform as output. When the capacitor is fully charged the output voltage across the resistor is zero. The arrival of the falling edge of the input waveform causes the capacitor to reverse charge giving a negative output spike, then as the square wave input changes during each cycle the output spike changes from a positive value to a negative value.

So, the output waveform would be like



(b) Calculate the I_{RMS}, I_D, ripple factor, rectification efficiency and PIV of rectifier circuit given below:



Ans. $N_1/N_2 = 1000/100 = 10$

RMS primary voltage= 220V

RMS secondary voltage = 220/10= 22 V

Max voltage across secondary= $22 \times \sqrt{2} = 21.11$ V

Max voltage appearing across half secondary winding is

= 31.11/2= 15.55 V

Max current appearing across half secondary winding

$= V_m / R_L = 15.55/1 = 15.55$mA

$I_{RMS} = I_m / \sqrt{2} = 15.55/\sqrt{2} = \mathbf{10.99\ mA}$

$I_{dc} = 2I_m / \pi = 2 \times 15.55/\pi = \mathbf{9.9\ mA}$

ripple factor $= \sqrt{(1.11)^2 - 1} = \mathbf{48\%}$

rectification efficiency $= 8/\pi^2 = \mathbf{81.06\ \%}$

PIV= $2V_m = 2 \times 15.55 = \mathbf{31.11\ V}$

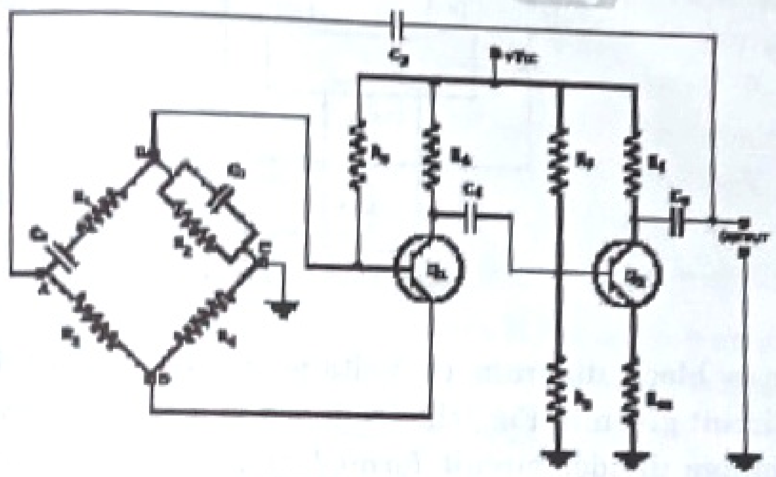
Q.3(a) Describe the working of Wien bridge oscillator circuit.

Ans. This oscillator circuit uses the Wien bridge to provide feedback with the desired phase shift. It gives highly stable oscillation frequency and does not vary much with supply or temperature variation.

It is basically a two-stage amplifier that consists of an RC bridge circuit or we can say Wien bridge circuit. The Wien bridge feedback net- work is used so as to make the oscillator sensitive to signal of only a particular frequency.

At this particular frequency, the Wien bridge gets balanced and provide's a phase shift of 0°. If Wien bridge feedback is not employed, then it will lead to poor frequency stability due to direct coupling. The Wien bridge circuit that we use is a lead-lag network as with the rise in fre- quency phase shift lags and with the reduction in frequency, it leads.

1 MHz is the maximum output frequency that is provided by this oscillator circuit. In a bridge circuit, the output produced will be in phase with the input only when the bridge is in the balanced condition.



Wien Bridge Oscillator Circuit Diagram

Construction of Wien Bridge Oscillator : Now, let's have a look at the circuit diagram of Wien bridge oscillator. The circuit mainly comprised of two transistors Q_1 and Q_2 and Wien bridge circuit in which a series RC circuit comprising of R_1C_1 is connected with a parallel RC circuit consist- ing of R_2C_2.

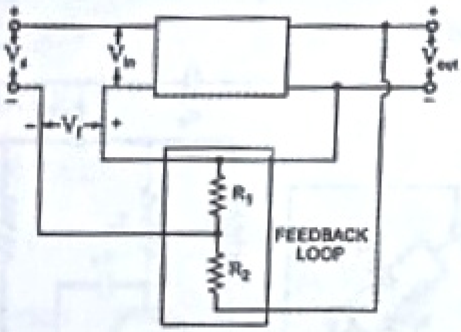
At low-frequency range, the reactance of serially connected capacitor C_1 is very high due to which it acts as an open circuit that results in blocking of an input signal which resultantly gives no signal at the output.

Similarly, at a higher frequency, the reactance of parallel capacitor C_2 becomes very low thus behaving like a short circuit across the output, which again results in no signal at the output.

So, there is a need to choose a frequency point in between the above two conditions that we have discussed right now so that we can achieve the maximum value at the output.

(b) Draw the circuit diagram of voltage-series feedback amplifier and derive the expression of closed-loop voltage gain.

Ans. Voltage Series Feedback Amplifier Circuit is also called the shunt-derived series-fed feedback. Here the amplifier and feedback network are connected in series-parallel. A fraction of the output voltage is applied in series opposition to the input voltage through feedback network, as shown in Fig.



Voltage-Series Feedback Circuit

In a block diagram of Voltage Series Feedback Amplifier Circuit given in Fig., the feedback voltage is derived from the voltage divider circuit formed of resistors R_1 and R_2. Thus feedback voltage is given as

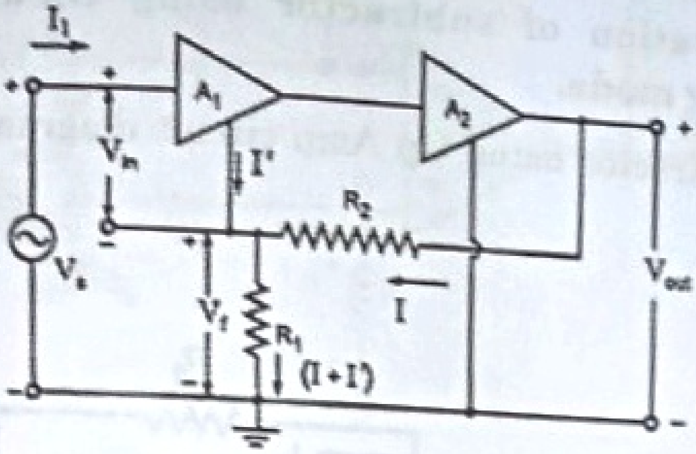
$$V_f = \beta V_{out} = \frac{R_1}{R_1 + R_2} V_{out}$$

Thus

$$\beta = \frac{R_1}{R_1 + R_2}$$

As seen, the input impedance of the amplifier and output impedance of the feedback network appear in series to the input and therefore input impedance to the amplifier is increased by a factor $(1 + \beta A)$.

Similarly input to the feedback network and output of the amplifier appear in parallel to the amplifier output. Thus, so far as V_{out} is concerned, output impedance of the amplifier is reduced, due to the shunting effect of the input to the feedback, by a factor $1/1 + \beta A$.



A general two stage amplifier having stage gains of A_1 and A_2 respectively is shown in Fig. The output of the second stage is fed back through the feedback network R_1R_2 in opposition to the input signal voltage V_s. Obviously this circuit is a case of voltage-series negative feedback. It is expected that input impedance will increase, output impedance will decrease and voltage gain will be stabilized.

An approximate analysis can be made if the open-loop gain is assumed to be very large and $I' << 1$. Under such conditions, we have $V_{in} \approx 0$ for a finite V_{out}, and Supply voltage,

$$V_s \simeq V_f \simeq IR_1 = R_1 \frac{V_{out}}{R_1 + R_2}$$

Thus

$$\beta = \frac{R_1}{R_1 + R_2}$$

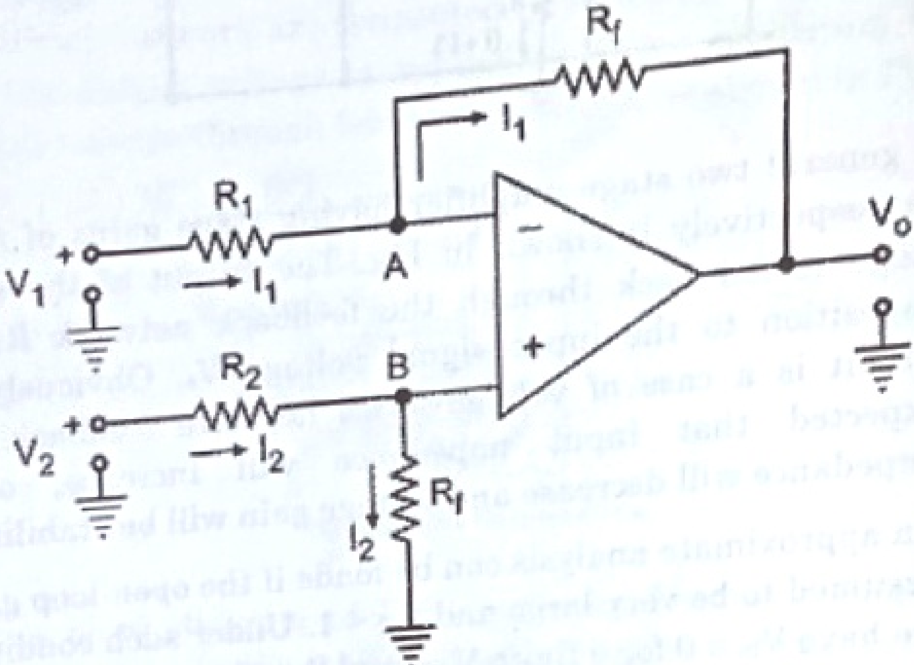
and overall gain with feedback,

$$A_f = \frac{V_{out}}{V_s} = \frac{R_1 + R_2}{R_1} = \frac{1}{\beta}$$

From the above equation it is obvious that under the above conditions the voltage gain is independent of all parameters except R_1 and R_2. Thus, if these resistors are stable, the circuit amplification is stabilized.

4. **Op-amp can be used to subtract the DC voltages (subtraction operation). Draw the circuit and explain the operation of subtractor using Op-amp in non-inverting mode.**

Ans. The Subtractor using Op Amp circuit diagram is shown in the Fig.



Subtractor circuit

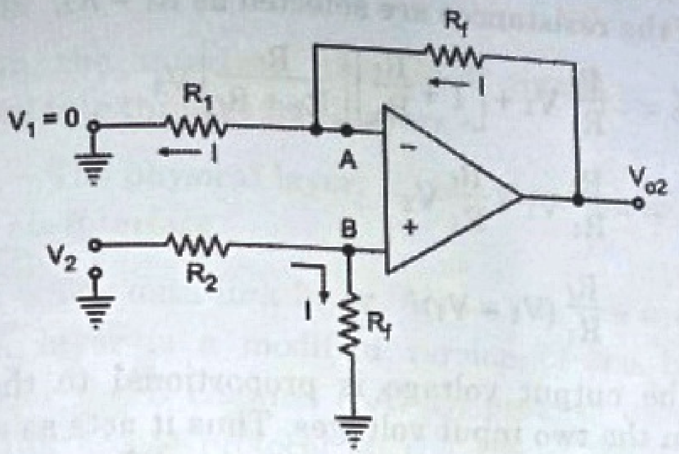
To find the relation between the inputs and output let us use Superposition principle.

Let V_{01} be the output, with input V_1 acting, assuming V_2 to be zero. And V_{02} be the output, with input V_2 acting, assuming V_1 to be zero.

With V_2 zero, the circuit acts as an inverting amplifier. Hence we can write

$$V_{01} = -\frac{R_f}{R_1} V_1 \quad \text{...(1)}$$

While with V_1 as zero, the circuit reduces to as shown in the Fig.



Let potential of node B be V_B. The potential of node A is same as B i.e. $V_A = V_B$. Applying voltage divider rule to the input V_2 loop,

$$V_B = \frac{R_f}{R_2 + R_f} \quad ...(2)$$

$$I = \frac{V_A}{R_1} = \frac{V_B}{R_1} \quad ...(3)$$

$$I = \frac{V_{02} - V_A}{R_f} = \frac{V_{02} - V_B}{R_f} \quad ...(4)$$

Equating the equations (3) and (4),

$$\frac{V_B}{R_1} = \frac{V_{02} - V_B}{R_f}$$

$$V_{02} = \frac{R_1 + R_f}{R_1} V_B$$

$$V_{02} = \left[1 + \frac{R_f}{R_1}\right] V_B \quad ...(5)$$

Substituting V_B from (2) in (5) we get,

$$V_{02} = \left[1 + \frac{R_f}{R_1}\right]\left[\frac{R_f}{R_2 + R_f}\right] V_2 \quad ...(6)$$

Hence using Superposition principle,

$$V_0 = V_{01} + V_{02}$$

$$= -\frac{R_f}{R_1} V_1 + \left[1 + \frac{R_f}{R_1}\right]\left[\frac{R_f}{R_2 + R_f}\right] V_2 \quad ...(7)$$

Now if the resistances are selected as $R_1 = R_2$,

$$V_0 = -\frac{R_f}{R_1}V_1 + \left[1 + \frac{R_f}{R_1}\right]\left[\frac{R_f}{R_2 + R_f}\right]V_2 \quad ...(7)$$

$$= -\frac{R_f}{R_1}V_1 + \frac{R_f}{R_1}V_2$$

$$V_0 = +\frac{R_f}{R_1}(V_2 - V_1) \quad ...(8)$$

Thus the output voltage is proportional to the difference between the two input voltages. Thus it acts as a Subtractor using Op Amp circuit or difference amplifier.

If $R_1 = R_2 = R_f$ is selected,

$$V_0 = V_2 - V_1 \quad ...(9)$$

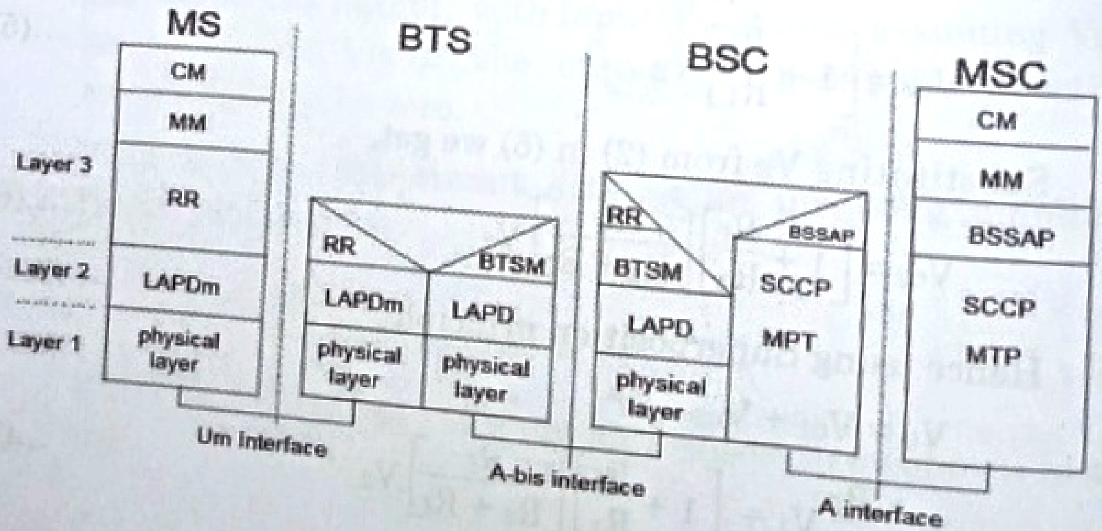
But by selecting proper values of R_1, R_2 and R_f, we can have the subtraction of two inputs with appropriate strengths like

$$V_0 = aV_2 - b\,V_1$$

5.(a) Draw and explain the GSM signalling protocol architecture.

Ans. GSM architecture is a layered model that is designed to allow communications between two different systems. The lower layers assure the services of the upper-layer protocols. Each layer passes suitable notifications to ensure the transmitted data has been formatted, transmitted, and received accurately.

The GMS protocol stacks diagram is shown below –



MS Protocols

Based on the interface, the GSM signaling protocol is assembled into three general layers –

Layer 1 – The physical layer. It uses the channel structures over the air interface.

Layer 2 – The data-link layer. Across the Um interface, the data-link layer is a modified version of the Link access protocol for the D channel (LAP-D) protocol used in ISDN, called Link access protocol on the Dm channel (LAP-Dm). Across the A interface, the Message Transfer Part (MTP), Layer 2 of SS7 is used.

Layer 3 – GSM signalling protocol's third layer is divided into three sub layers –

- Radio Resource Management (RR),
- Mobility Management (MM), and
- Connection Management (CM).

MS to BTS Protocols

The RR layer is the lower layer that manages a link, both radio and fixed, between the MS and the MSC. The MM layer is stacked above the RR layer. It handles the functions that arise from the mobility of the subscriber, as well as the authentication and security aspects. The CM layer is the topmost layer of the GSM protocol stack. This layer is responsible for Call Control, Supplementary Service Management, and Short Message Service Management.

BSC Protocols

The BSC uses a different set of protocols after receiving the data from the BTS. The Abis interface is used between the BTS and BSC. At this level, the radio resources at the lower portion of Layer 3 are changed from the RR to the Base Transceiver Station Management (BTSM). The BTS management layer is a relay function at the BTS to the BSC.

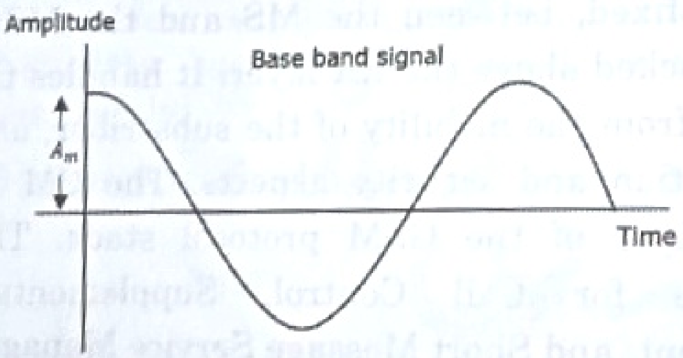
MSC Protocols

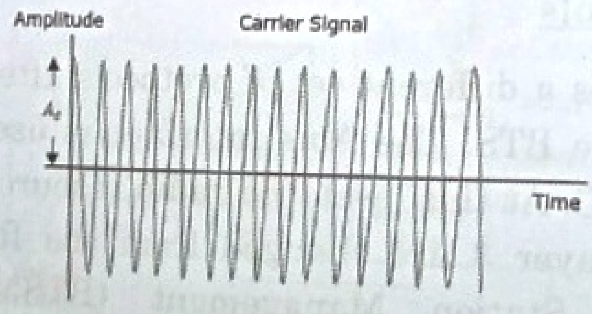
At the MSC, starting from the BSC, the information is mapped across the A interface to the MTP Layers 1 through 3. Here, Base Station System Management Application Part (BSS MAP) is said to be the equivalent set of radio resources

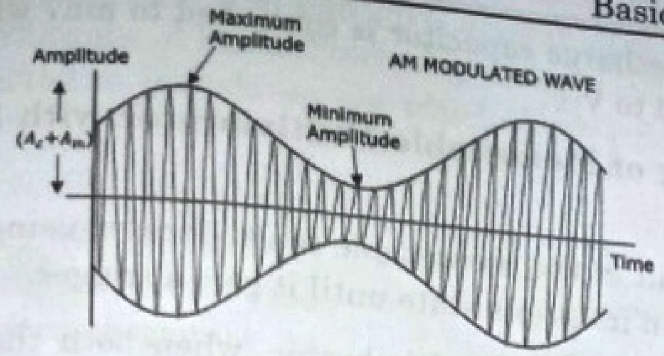
(b) What is the need of modulation? Draw the wave shape of modulating signal, carrier signal and modulated wave in amplitude modulation.

Ans. Need for modulation: The baseband signals can be transmitted directly, but the baseband transmission has many limitations which can be overcome using modulation. In the process of modulation, the baseband signal is translated i.e. shifted from low frequency to high frequency, which doesn't affect the parameters of the modulating signal.

Amplitude Modulation: The amplitude of the carrier signal varies in accordance with the instantaneous amplitude of the modulating signal." Which means, the amplitude of the carrier signal containing no information varies as per the amplitude of the signal containing information, at each instant.



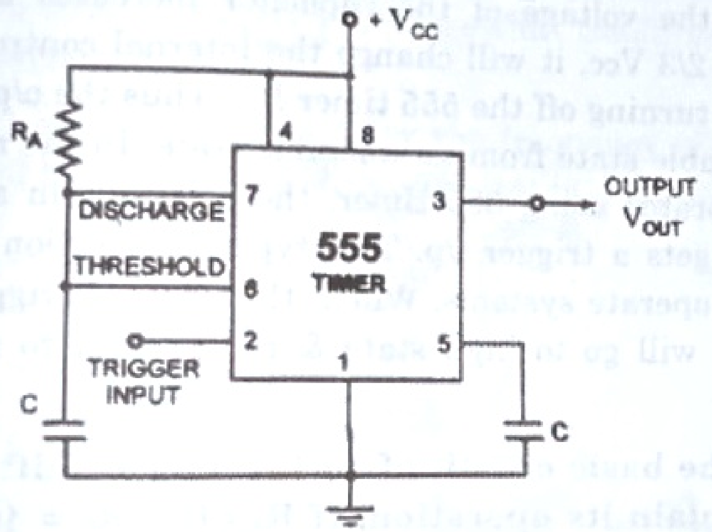




The first figure shows the modulating wave, which is the message signal. The next one is the carrier wave, which is a high frequency signal and contains no information. While, the last one is the resultant modulated wave.

6.(a) Draw the functional block diagram and explain the operation of Monostable multi-vibrator using IC 555 timer.

Ans.



In the above circuit, the pin1 is connected to the ground and the trigger input is given to the pin2.In inactive condition of o/p, this i/p is kept at +Vcc. To get transition of the output from a stable state to unstable state, a negative going pulse of narrow width and amplitude of greater than +2/3 Vcc is applied to pin2. The o/p is taken from pin3 and pin4 is connected to +Vcc to avoid accidental reset.Pin5 is connected to the ground via a 0.01uF capacitor to avoid noise. Pin6 and pin7 are shorted and a resistor is connected between pins 6

& 8. A discharge capacitor is connected to pin7 while pin8 is connected to Vcc.

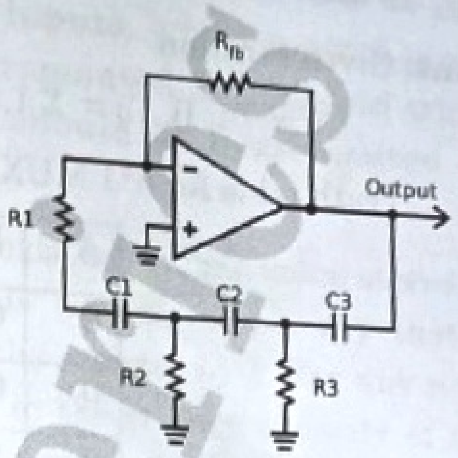
Working of Monostable Multivibrator with 555 Timer Circuit

- The output of the monostable multivibrator using 555 timer remains in its stable state until it gets a trigger.
- In monostable 555 multivibrator, when both the transistor and capacitor are shorted then this state is called as a stable state.
- When the voltage goes below at the second pin of the 555 IC, the o/p becomes high. This high state is called quasi stable state. When the circuit activates then the transition from a stable state to quasi stable state.
- Then the discharge transistor is cut off and capacitor starts charging to VCC. Charging of the capacitor is done via the resistor R1 with a time constant R1C1
  Hence, the voltage of the capacitor increases and finally exceeds 2/3 Vcc, it will change the internal control flip flop, thereby turning off the 555 timer IC. Thus the o/p goes back to its stable state from an unstable state. In the monostable multivibrator using 555 timer, the o/p stays in a low state until it gets a trigger i/p. This type of operation is used in push to operate systems. When the input is triggered, then the o/p will go to high state & comes back to its original state.

(b) Draw the basic circuit of an R-C phase-shift oscillator and explain its operation. If $R_1 = R_2 = R_3 = 400$ kΩ and $C_1 = C_2 = C_3 = 50$ pF, determine the frequency of oscillation in phase-shift oscillator.

Ans. RC phase-shift oscillators use resistor-capacitor (RC) network (Figure 1) to provide the phase-shift required by the feedback signal. They have excellent frequency stability and can yield a pure sine wave for a wide range of loads. RC phase-shift oscillator circuit can be built with a resistor as well as a capacitor. This circuit offers the required phase shift with the feedback signal. They have outstanding frequency strength and can give a clean sine wave for an extensive range of loads. Preferably an easy RC network can be expected to include an o/p which directs the input with 90°.

However, in reality, the phase-difference will be less than this as the capacitor used in the circuit cannot be ideal. Mathematically the phase angle of the RC network is expressed as



$$\varphi = \tan^{-1} \frac{X_C}{R}$$

Where, $X_C = 1/(2\pi fC)$ is the reactance of the capacitor C and R is the resistor. In oscillators, these kind of RC phase-shift networks, each offering a definite phase-shift can be cascaded so as to satisfy the phase-shift condition led by the Barkhausen Criterion.

The generalized expression for the frequency of oscillations produced by a RC phase-shift oscillator is given by

$$f = \frac{1}{2\pi RC\sqrt{2N}}$$

Here, $R = R_1 = R_2 = R_3 = 400K\Omega$

$C = C_1 = C_2$

$= C_3 = 50pF$

Here, N specifies the number of RC stages connected in the feedback phase network. 2N is directly substituted as 6 because there are fixed 3 of RC stages.

Put the values in equation

$$f = \frac{1}{2 \times 3.14 \times 400 \times 10^3 \times 50 \times 10^{-12} \times 2.449}$$

$f = 325.10$ Hz

7. (a) Implement the function

F(A, B, C) = Σ 1, 3, 4, 6, 7

using 8 × 1 MUX. Use A, B and C as selection line in which C is LSB and A is MSB.

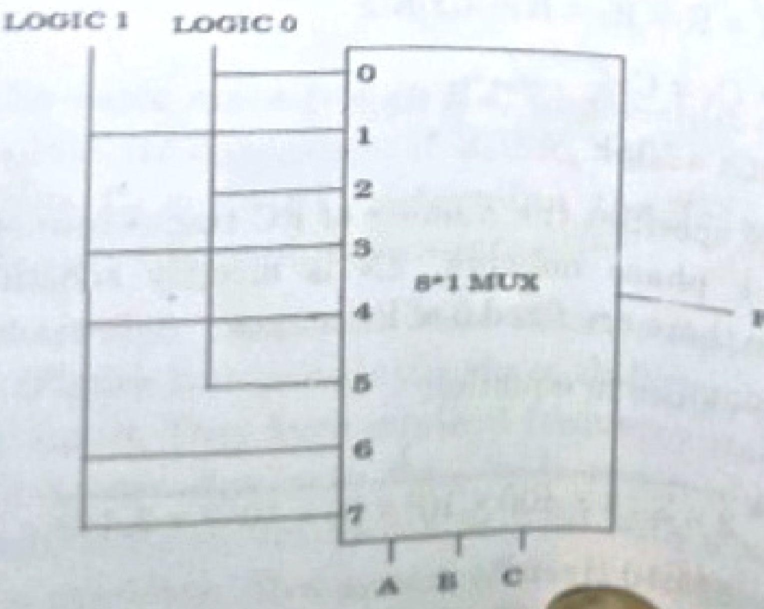
Ans. Given function

F = (A, B, C) = Σ 1,3,4,6,7

Truth table for 8*1 MUX using three variables A, B, C.

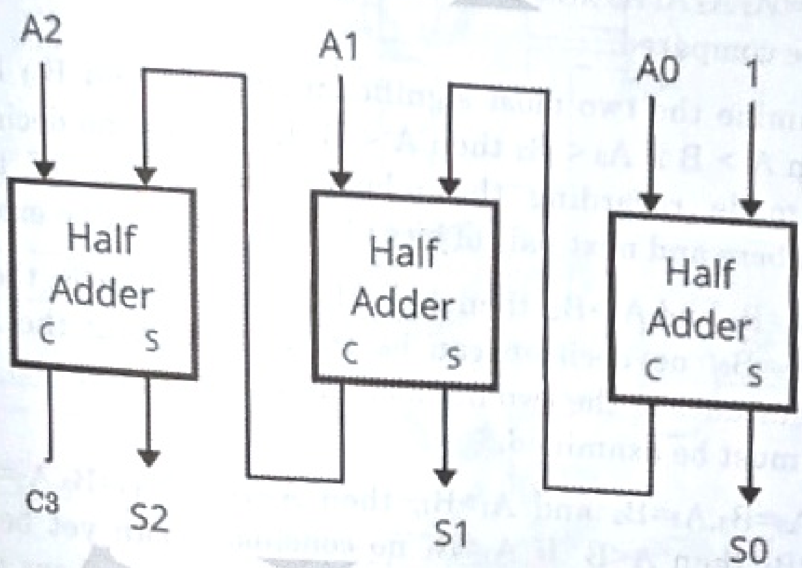
A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

Implementation of function using 8*1 MUX

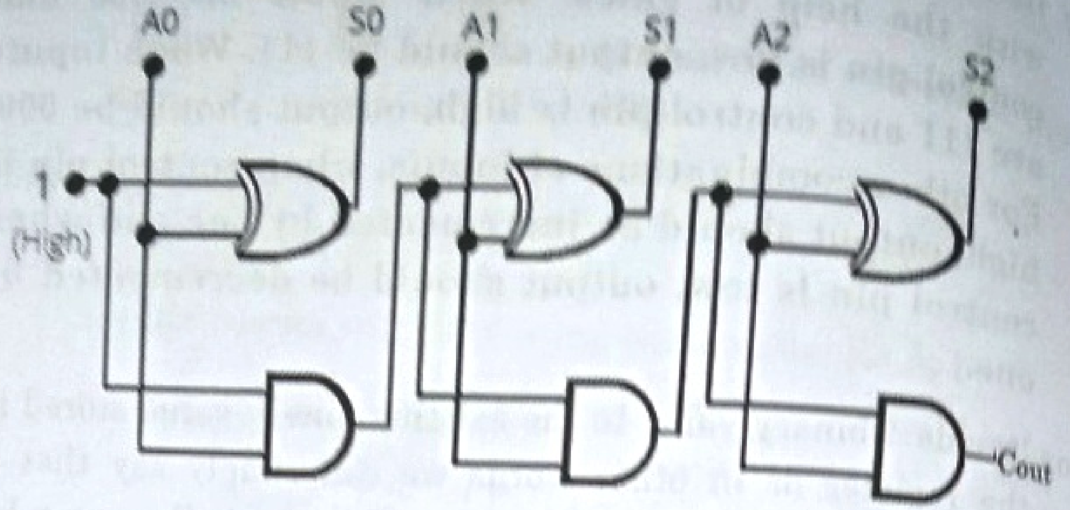


(b) **Design 3-bit binary incrementer/decrementer circuit with the help of gates. When inputs are 000 and control pin is low, output should be 111. When inputs are 111 and control pin is high, output should be 000. For other combinations of inputs, when control pin is high, output should be incremented by one and when control pin is low, output should be decremented by one.**

Ans. It adds 1 binary value to the existing binary value stored in the register or in other words we can simply say that it increases the value stored in the register by 1. For any n-bit binary incrementer ,'n' refers to the storage capacity of the register which needs to be incremented by 1. So we require 'n' number of half adders . Thus, in case of 3 bit binary incrementer we require 3 half adders.



The half adders are connected one after the other , as it has 2 inputs and 2 outputs , so for the LSB (least significant bit) half adder or the right most half adder is given 1 as direct input(first input) and A0 which is the first bit of the register (second input) , so we get the two output : sum (S0) and carry (C). The carry(C) from previous half adder is propagated to the next half adder, so the carry output of the previous half adder becomes the input of the next higher order half adder.



8.(a) Design a combinational circuit to check that two numbers A =($A_3A_2A_1A_0$) and B = ($B_3B_2B_1B_0$) are equal with the help of gates. Output should be indicated by X. Output line X should be high if A = B.

Ans. A = $A_3 A_2 A_1 A_0$ and B = $B_3 B_2 B_1 B_0$ be the two 4- bit numbers to be compared.

1) Examine the two most significant bits (A_3 and B_3) If $A_3>B_3$ then A > B if $A_3 < B_3$ then A < B. If $A_3 = B_3$, no decision can be made regarding the relative magnitudes of the two numbers and next pair of bits (A_2 and B_2) must be examined.

2) If $A_3=B_3$ and $A_2>B_2$, then A>B, if $A_3=B_3$ and $A_2<B_2$ then A<B. If $A_2=B_2$, no decision can be made regarding the relative magnitudes of the two numbers and next pair of bits (A_1 and B_1) must be examined.

3) If $A_3=B_3$,$A_2=B_2$ and $A_1>B_1$, then A>B, If $A_3=B_3$,$A_2=B_2$ and $A_1<B_1$ then A<B .If $A_1=B_1$ no conclusion can yet be drawn regarding the relative magnitudes of two numbers and the LSBs (A_0 and B_0) must be examined.

4) If $A_3=B_3$,$A_2=B_2$,$A_1=B_1$

and $A_0>B_0$, then A > B , if $A_3=B_3$, $A_2=B_2$, $A_1=B_1$ and $A_0<B_0$ then A<B. If $A_0 = B_0$, then A = B.

If the digits are equal (i.e. $A_3 = B_3 = 0$ or $A_3 = B_3 = 1$), then

$$X_3 = \overline{A}_3 \overline{B}_3 + A_3B_3 = \overline{A_3 (+) B_3}$$

$$X_2 = \bar{A}_2\bar{B}_2 + A_2B_2 = \overline{A_2 (+) B_2}$$

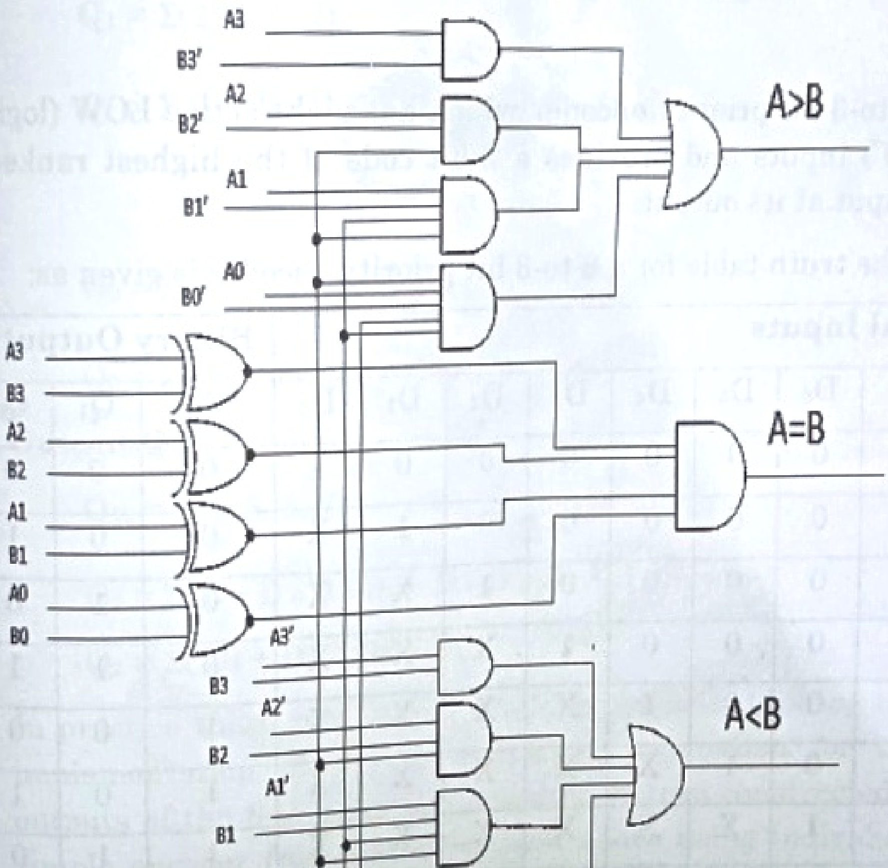
$$X_1 = \bar{A}_1\,\bar{B}_1 + A_1B_1 = \overline{A_1 (+) B_1}$$

$$X_0 = \bar{A}_0\,\bar{B}_0 + A_0B_0 = \overline{A_0 (+) B_0}$$

$$X = X_3X_2X_1\,X_0$$

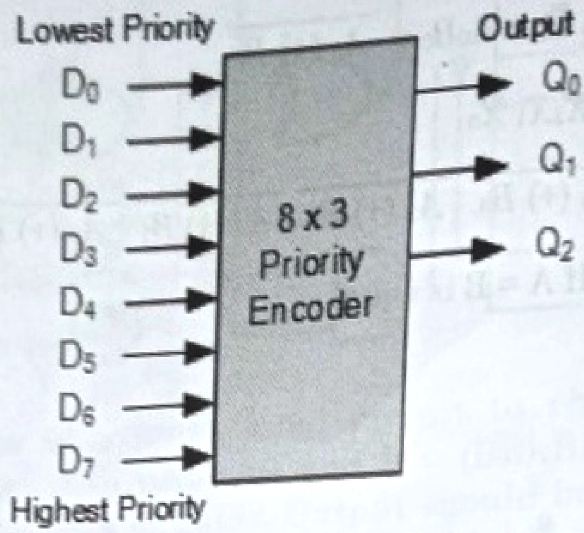
$$= \overline{A_3 (+) B_3}\;\; \overline{A_2 (+) B_2}\;\; \overline{A_1 (+) B_1}\;\; \overline{A_0 (+) B_0}$$

X = 1 If A = B is equal



(b) Design 8 × 3 priority encoder with the help of basic gates.

Ans.



8-to-3 bit priority encoder which has eight active LOW (logic "0") inputs and provides a 3-bit code of the highest ranked input at its output.

The truth table for a 8-to-3 bit priority encoder is given as:

Digital Inputs								Binary Output		
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Q_2	Q_1	Q_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	X	0	0	1
0	0	0	0	0	1	X	X	0	1	0
0	0	0	0	1	X	X	X	0	1	1
0	0	0	1	X	X	X	X	1	0	0
0	0	1	X	X	X	X	X	1	0	1
0	1	X	X	X	X	X	X	1	1	0
1	X	X	X	X	X	X	X	1	1	1

Where X equals "dont care", that is it can be at a logic "0" level or at a logic "1" level. From this truth table, the

Boolean expression for the encoder above with data inputs D0 to D7 and outputs Q0, Q1, Q2 is given as:

Output Q_0

$$Q_0 = \Sigma(1, 3, 5, 7)$$

$$Q_0 = \Sigma(\bar{D}_7 \bar{D}_6 \bar{D}_5 \bar{D}_4 \bar{D}_3 \bar{D}_2 \bar{D}_1 + \bar{D}_7 \bar{D}_6 \bar{D}_5 \bar{D}_4 D_3 + \bar{D}_7 \bar{D}_6 D_5 D_7)$$

$$Q_0 = \Sigma(\bar{D}_6 \bar{D}_4 \bar{D}_2 D_1 + \bar{D}_6 \bar{D}_4 D_3 + \bar{D}_6 D_5 + D_7)$$

$$Q_0 = \Sigma(\bar{D}_6 (\bar{D}_4 \bar{D}_2 D_1 + \bar{D}_4 D_3 + D_5) + D_7)$$

Output Q_1

$$Q_1 = \Sigma(2, 3, 6, 7)$$

$$Q_1 = \Sigma(\bar{D}_7 \bar{D}_6 \bar{D}_5 \bar{D}_4 \bar{D}_3 D_2 + \bar{D}_7 \bar{D}_6 \bar{D}_5 \bar{D}_4 D_3 + \bar{D}_7 \bar{D}_6 D_7)$$

$$Q_0 = \Sigma(\bar{D}_5 \bar{D}_4 D_2 + \bar{D}_5 \bar{D}_4 D_3 + D_6 D_7)$$

$$Q_0 = \Sigma(\bar{D}_5 (\bar{D}_4 (D_2 + D_3) + D_6 + D_7)$$

Output Q2

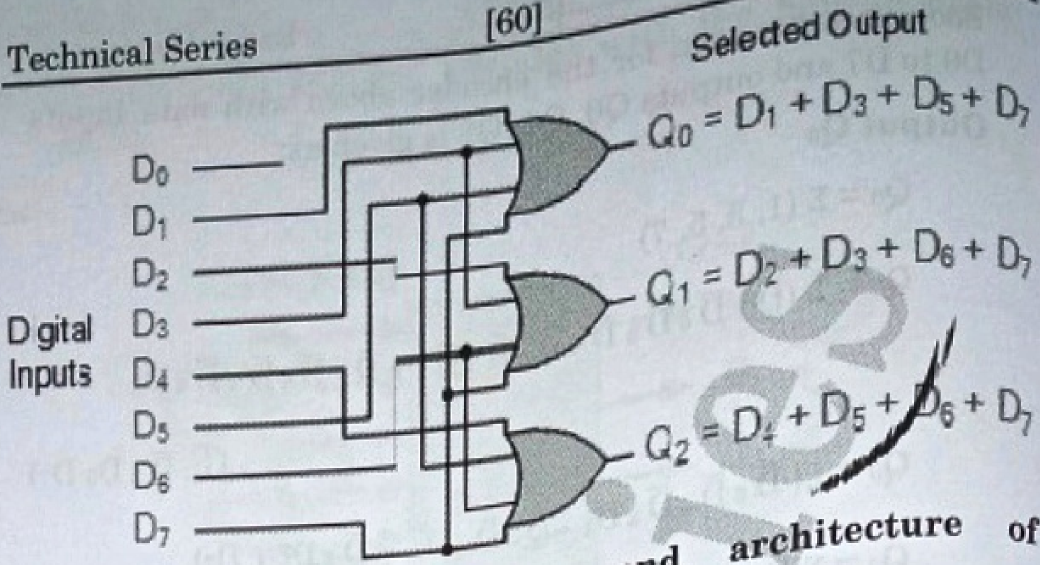
$$Q_{12} = \Sigma(4, 5, 6, 7)$$

$$Q_2 = \Sigma(\bar{D}_7 \bar{D}_6 \bar{D}_5 D_4 + \bar{D}_7 \bar{D}_6 D_5 + \bar{D}_7 D_6 + D_7)$$

$$Q_2 = \Sigma(D_4 + D_5 + D_6 + D_7)$$

In practice these zero inputs would be ignored allowing the implementation of the final Boolean expression for the outputs of the 8-to-3 priority encoder. We can constructed a simple encoder from the expression above using individual OR gates as follows.

Digital Encoder using Logic Gates



9.(a) Compare the function and architecture of Microprocessor and Microcontroller.

Ans. Difference Between Microprocessor and Microcontroller

Microprocessor	Microcontroller
Microprocessor is the heart of Computer system.	Micro Controller is the heart of an embedded system.
It is only a processor, so memory and I/O components need to be connected externally	Micro Controller has a processor along with internal memory and I/O components.
Memory and I/O has to be connected externally, so the circuit becomes large.	Memory and I/O are already present, and the internal circuit is small.
You can't use it in compact systems	You can use it in compact systems.
Cost of the entire system is high	Cost of the entire system is low
Due to external components, the total power consumption is high. Therefore, it is not ideal for the devices running on stored power like batteries.	As external components are low, total power consumption is less. So it can be used with devices running on stored power like batteries.
Most of the microprocessors do	Most of the microcontrollers

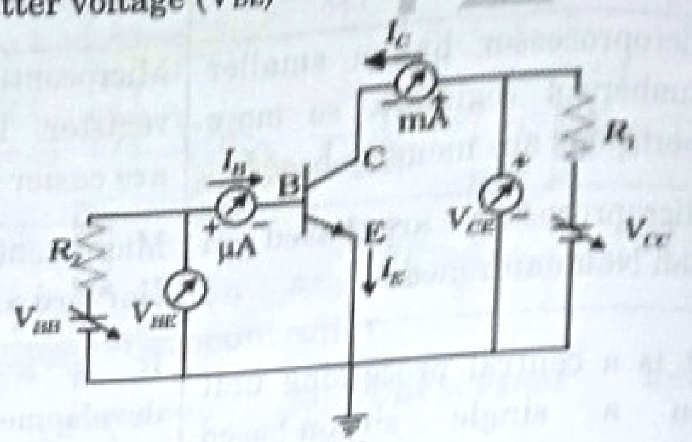
Microprocessor	Microcontroller
not have power saving features.	offer power-saving mode.
It is mainly used in personal computers.	It is used mainly in a washing machine, MP3 players, and embedded systems.
Microprocessor has a smaller number of registers, so more operations are memory-based.	Microcontroller has more register. Hence the programs are easier to write.
Microprocessors are based on Von Neumann model	Micro controllers are based on Harvard architecture
It is a central processing unit on a single silicon-based integrated chip.	It is a byproduct of the development of microprocessors with a CPU along with other peripherals.
It has no RAM, ROM, Input-Output units, timers, and other peripherals on the chip.	It has a CPU along with RAM, ROM, and other peripherals embedded on a single chip.
It uses an external bus to interface to RAM, ROM, and other peripherals.	It uses an internal controlling bus.
Microprocessor-based systems can run at a very high speed because of the technology involved.	Microcontroller based systems run up to 200MHz or more depending on the architecture.
It's used for general purpose applications that allow you to handle loads of data.	It's used for application-specific systems.
It's complex and expensive, with a large number of instructions to process.	It's simple and inexpensive with less number of instructions to process.

(b) Draw the input-output and transfer characteristics of CE amplifier.

Ans. In Common Emitter (CE) configuration, the emitter is the common terminal. Hence, the input is between the base and the emitter while the output is between the collector and the emitter.

Input characteristic – the variation of the base current (I_B) with the base-emitter voltage (V_{BE})

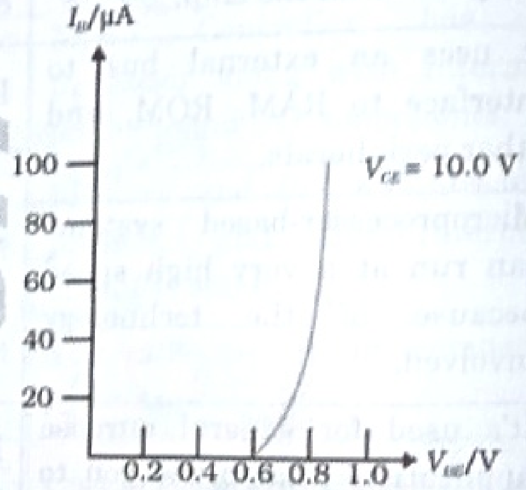
Output characteristic – the variation of the collector current (I_C) with the collector-emitter voltage (V_{CE})



It is observed that the output characteristics are controlled by the input characteristics. Hence, the collector current changes with the base current. Let's study them with the help of a circuit diagram shown below:

Input characteristic

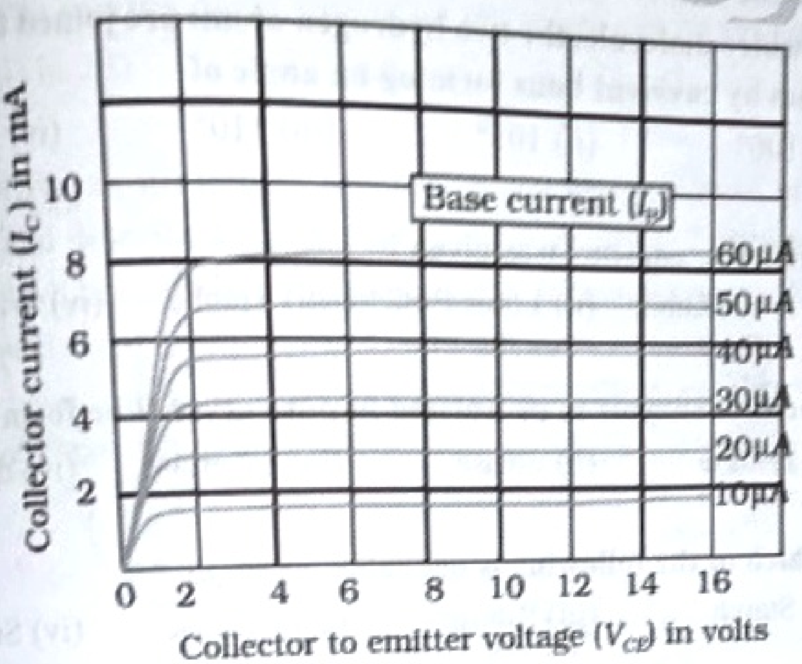
To study input characteristics, a curve is plotted between the base current (I_B) and the base-emitter voltage (V_{BE}) to study the input characteristics of the junction transistor in CE configuration. The collector-emitter voltage (V_{CE}) is kept at a fixed value to study the relation between I_B and V_{BE}. An increase in the value of V_{CE} appears as an increase in the value of V_{CB}



Output characteristic

To study the output characteristics, plot a curve is between the Collector current (I_C) and the collector-emitter voltage

(V_{CE}). Also, keep the base current (I_B) at a steady value. if the base-emitter current (V_{BE}) is increased by a small amount, we can observe an increase in hole current from the emitter and electron current from the base regions. Hence, I_B and I_C increase proportionally. Or, if I_B increases, I_C increases too. So, keeping I_B constant and plotting I_C against V_{CE}, we can make the following observations:



Transfer Characteristics:

Current Amplification Factor (β) is the ratio of change in the collector current (I_C) to the change in base current (I_B) when the collector-emitter voltage (V_{CE}) is kept constant. Also, the transistor is in an active state. Now, the small signal current gain is

$$\beta_{ac} = (\Delta I_C / \Delta I_B)_{VCE}$$